

# DEI1041

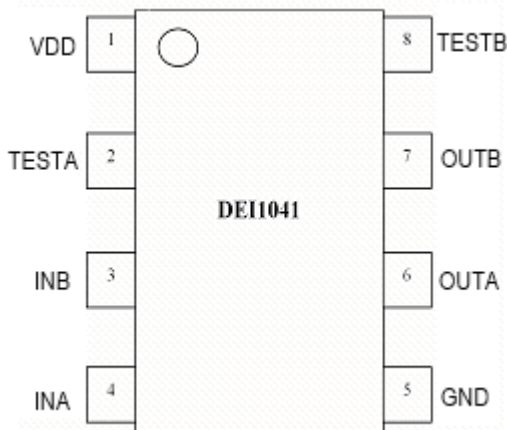
## ARINC 429 LINE RECEIVER

### FEATURES

- ARINC 429 to TTL/CMOS logic line receiver
- Operates from single +5V  $\pm$  10% or 3.3V  $\pm$  10%, -5% power supply
- ARINC inputs internally protected to lightning requirements of DO-160D Level A3
- Operates in high noise environment
  - Input Common Voltage Range:  $\pm$  20V
  - 2V minimum Input hysteresis
- Logic level TEST inputs bypass analog inputs.
- 8 Lead SOIC.
- Replacement for HI-8588 and HI-8588-10

### TERMINAL DESCRIPTION

Table 1 Terminal Description



NAME	DESCRIPTION
<b>INA</b>	<b>429 INPUT.</b> ARINC 429 format serial digital data "A" input.
<b>INB</b>	<b>429 INPUT.</b> ARINC 429 format serial digital data "B" input.
<b>TESTA</b>	<b>LOGIC INPUT.</b> Test input A.
<b>TESTB</b>	<b>LOGIC INPUT.</b> Test input B.
<b>OUTA</b>	<b>LOGIC OUTPUT.</b> CMOS/TTL format serial digital data "A" output.
<b>OUTB</b>	<b>LOGIC OUTPUT.</b> CMOS/TTL format serial digital data "B" output.
<b>VDD</b>	<b>POWER INPUT.</b> 5 VDC OR 3.3VDC.
<b>GND</b>	<b>POWER INPUT.</b> Ground.

## FUNCTIONAL DESCRIPTION

The DEI1041 is a BICMOS device which contains one ARINC 429 differential line receiver. It translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. It meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 “DEI1041 Block Diagram and Truth Table”.

The device is designed to operate in a high noise environment. Inputs are accepted over a +/- 20V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160D Level A3. The ARINC inputs may optionally be connected to ARINC bus through external 10k ohm series resistors. These resistors may be added in combination with transient voltage suppressors to achieve lightning protection beyond the Level A3 limits due to high input impedance.

The DEI1041 device provides logic level TEST inputs for built in system test. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.

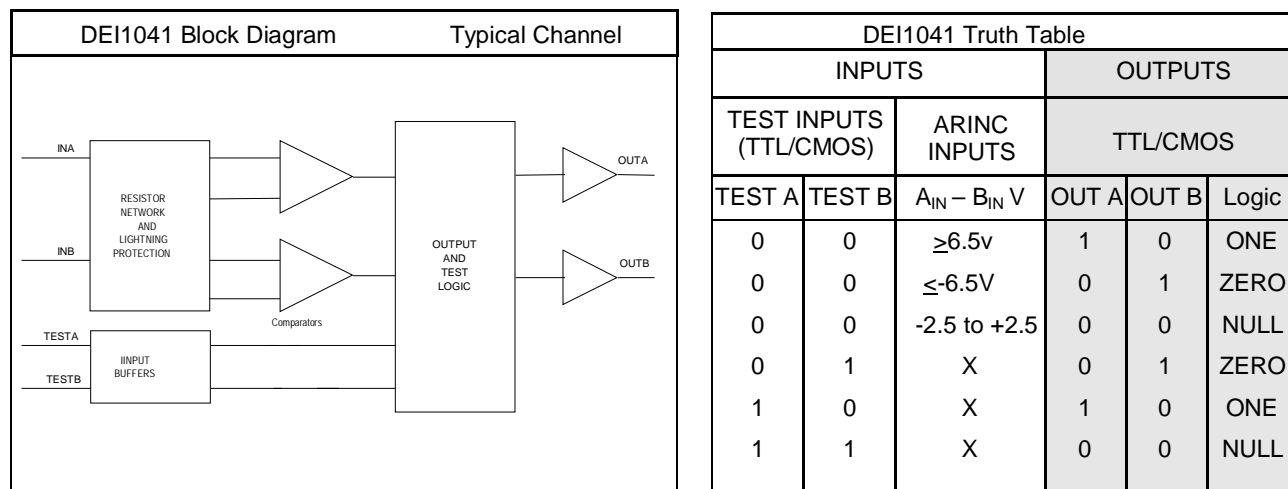


Figure 1 DEI1041 Block Diagram and Truth Table

## ELECTRICAL DESCRIPTION

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	Vdd	+5V $\pm$ 10% +3.3V +10%, -5%
Logic Input Levels	VTESTA,B	0 to Vdd
Operating Temperature	Ta	-55 to +85°C -55 to +125°C
-SES		
-SMS		

**Table 3 Absolute Maximum Rating**

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to V <sub>SS</sub> )	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)	-40	+40	V
Input Voltage (Test Inputs)	V <sub>SS</sub> - 0.3	V <sub>DD</sub> +0.3	V
Power Dissipation @ 85 °C		500	mW
Junction Temperature: T <sub>jmax</sub> , (limited by molding compound T <sub>g</sub> )		145	°C
Peak Body Temperature, - G Package		260	°C
Lightning Protection (ARINC 429 Channel Inputs) Waveform 3 (2) Waveform 4, 5A, 5B* (2) (3)	-600 -300	+600 +300	V V
ESD per JEDEC A114-A Human Body Model	-1000	1000	V

Notes:

1. Stresses above these limits can cause permanent damage.
2. Per DO160D, Sect 22 Level 3A. See Figures 4-6.
3. Inputs can be protected to withstand higher stress by adding series resistors and shunt TVS on inputs. Inputs withstand 1500V Waveform 5A when clipped ≤ 600V.

**Table 4 Electrical Characteristics**

**Conditions:** Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V<sub>DD</sub> = +5V ± 10% or 3.3V +10%, -5%

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
<b>ARINC INPUTS</b>						
V <sub>A</sub> - V <sub>B</sub> = Logic +1	OUTA = 1	V <sub>+1</sub>	6.5	10	13	V
V <sub>A</sub> - V <sub>B</sub> = Logic -1	OUTB = 1	V <sub>-1</sub>	-6.5	-10	-13	V
V <sub>A</sub> - V <sub>B</sub> = Logic Null	OUTA = 0 OUTB = 0	V <sub>NULL</sub>	-2.5	0	2.5	V
Input Hysteresis		V <sub>HY</sub>	2.0		4.0	V
V <sub>A</sub> - V <sub>B</sub> = Null to +1 transition	OUTA = 0→1	V <sub>T+1+</sub>	5.5		6.5	V
V <sub>A</sub> - V <sub>B</sub> = +1 to Null transition	OUTA = 1→0	V <sub>T+1-</sub>	2.5		3.5	V
V <sub>A</sub> - V <sub>B</sub> = Null to -1 transition	OUTB = 0→1	V <sub>T-1+</sub>	-6.5		-5.5	V
V <sub>A</sub> - V <sub>B</sub> = -1 to Null transition	OUTB = 1→0	V <sub>T-1-</sub>	-3.5		-2.5	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V <sub>CM</sub>	-20		+20	V
Input Resistance IN <sub>A</sub> to IN <sub>B</sub>	V <sub>DD</sub> open, Shorted to V <sub>SS</sub> or +5V (1)	R <sub>IN</sub>	280k	780K		Ω
Input Resistance IN <sub>A</sub> or IN <sub>B</sub> to V <sub>SS</sub>	V <sub>DD</sub> open, Shorted to V <sub>SS</sub> or +5V	R <sub>S</sub>	140k	390K		Ω
Input Capacitance IN <sub>A</sub> to IN <sub>B</sub>	V <sub>DD</sub> open, Shorted to V <sub>SS</sub> or +5V (1)	C <sub>IN</sub>			10	pF
Input Capacitance IN <sub>A</sub> or IN <sub>B</sub> to V <sub>SS</sub>	V <sub>DD</sub> open, Shorted to V <sub>SS</sub> or +5V (1)	C <sub>S</sub>			10	pF

**Conditions:** Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V<sub>DD</sub> = +5V ± 10% or 3.3V +10%, -5%

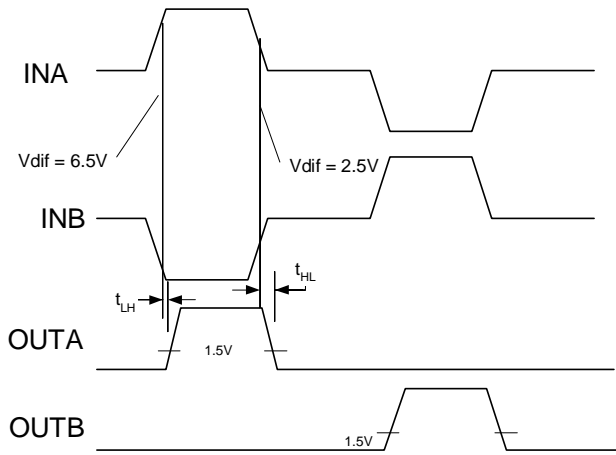
PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
<b>TEST INPUTS</b>						
Logic 0 Voltage		V <sub>IL</sub>			0.8	V
Logic 1 Voltage		V <sub>IH</sub>	2.0			V
Logic 0 Current	V <sub>IL</sub> = 0.8	I <sub>IL</sub>			20	μA
Logic 1 Current	V <sub>IH</sub> = 2.0	I <sub>IH</sub>			25	μA
<b>LOGIC OUTPUTS</b>						
OUT A or OUT B	I <sub>OH</sub> = 5mA (VDD=5V) I <sub>OH</sub> = 1.5mA (VDD=3.3V) TTL Compatible	V <sub>OH</sub>	2.4			V
OUT A or OUT B	I <sub>OL</sub> = 5mA (VDD=5V)	V <sub>OL</sub>			0.5	V
	I <sub>OL</sub> = 1.5mA (VDD=3.3V)				0.4	
	TTL Compatible					
OUT A or OUT B	I <sub>OH</sub> = 100μA CMOS Compatible	V <sub>OH</sub>	V <sub>DD</sub> - 50mV			V
OUT A or OUT B	I <sub>OL</sub> = 100μA CMOS Compatible	V <sub>OH</sub>			V <sub>SS</sub> + 50mV	V
<b>SUPPLY CURRENT</b>						
V <sub>DD</sub> Current	Data Rate = 0MHz, A/BIN =open, A/BOUT=open, Vdd = 5.5V or 3.63V	I <sub>DD</sub>		2.5	5	mA

Notes:

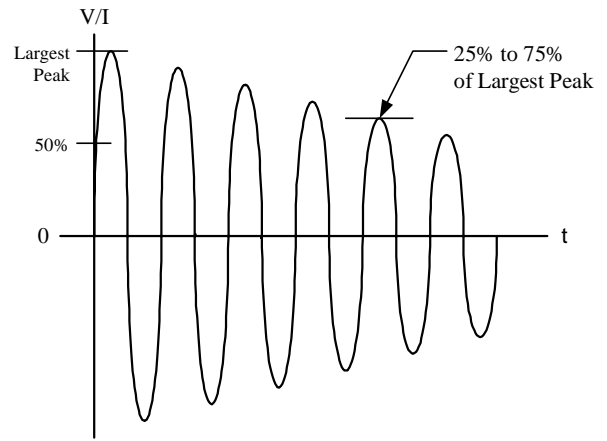
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to Ground unless otherwise noted.

**Table 5 Switching Characteristics**

PARAMETER	TEST CONDITION	SYMBOL	MAX	MAX	UNITS
			Vdd 3.3V	Vdd 5V	
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C <sub>L</sub> = 50pF	t <sub>LH</sub>	1000	900	ns
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C <sub>L</sub> = 50pF	t <sub>HL</sub>	1000	900	ns
Matching of t <sub>LH</sub> and t <sub>HL</sub>		Dtp	500	500	ns
OUT A/B rise time	10% to 90%, C <sub>L</sub> = 50pF	t <sub>r</sub>	50	25	ns
OUT A/B fall time	10% to 90%, C <sub>L</sub> = 50pF	t <sub>f</sub>	50	25	ns
TESTA/B to OUTA/B Prop delay	C <sub>L</sub> = 50pF	t <sub>TOH</sub>	100	60	ns
TESTA/B to OUTA/B Prop delay	C <sub>L</sub> = 50pF	t <sub>TOL</sub>	100	60	ns

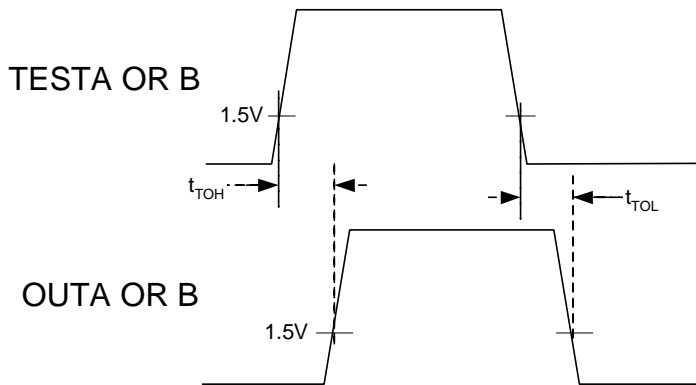


**Figure 2 ARINC 429 Input to Logic Output Switching Waveform**

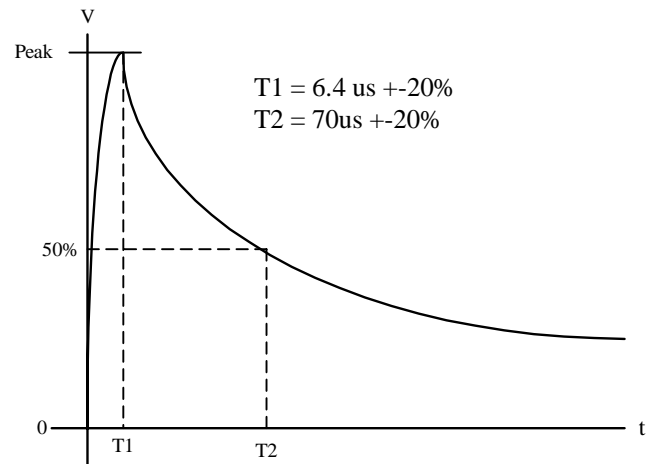


**Figure 4 DO160D Lightning Induced Transient Voltage Waveform #3.**

Voc = 600V, Isc = 24A, Frequency = 1MHz  $\pm$ 20%



**Figure 3 TEST Input to Logic Output Switching Waveform**

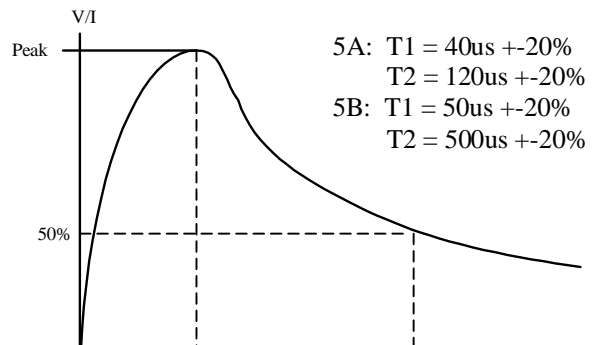


**Figure 5 DO160D Lightning Induced Transient Voltage Waveform #4.**

Voc = 300V, Isc = 60A

**LIGHTNING TRANSIENT NOTES:**

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.



**Figure 6 DO160D Lightning Induced Transient Voltage Waveform #5.**

Voc = 300V, Isc = 300A

# PACKAGE DESCRIPTION

## 8 Lead NB SOIC

Table 6 - 8 Lead NB SOIC Package Characteristics

Table 6: Package Characteristics Table	
<b>PACKAGE TYPE</b>	<b>16 Lead SOIC Narrow Body, Green</b>
REFERENCE	8L NB SOIC G
<b>THERMAL RESISTANCE:</b>	
$\theta_{JA}$ (4 layer PCB with Power Planes)	55 °C/W
$\theta_{JC}$	24 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MS-012-AC

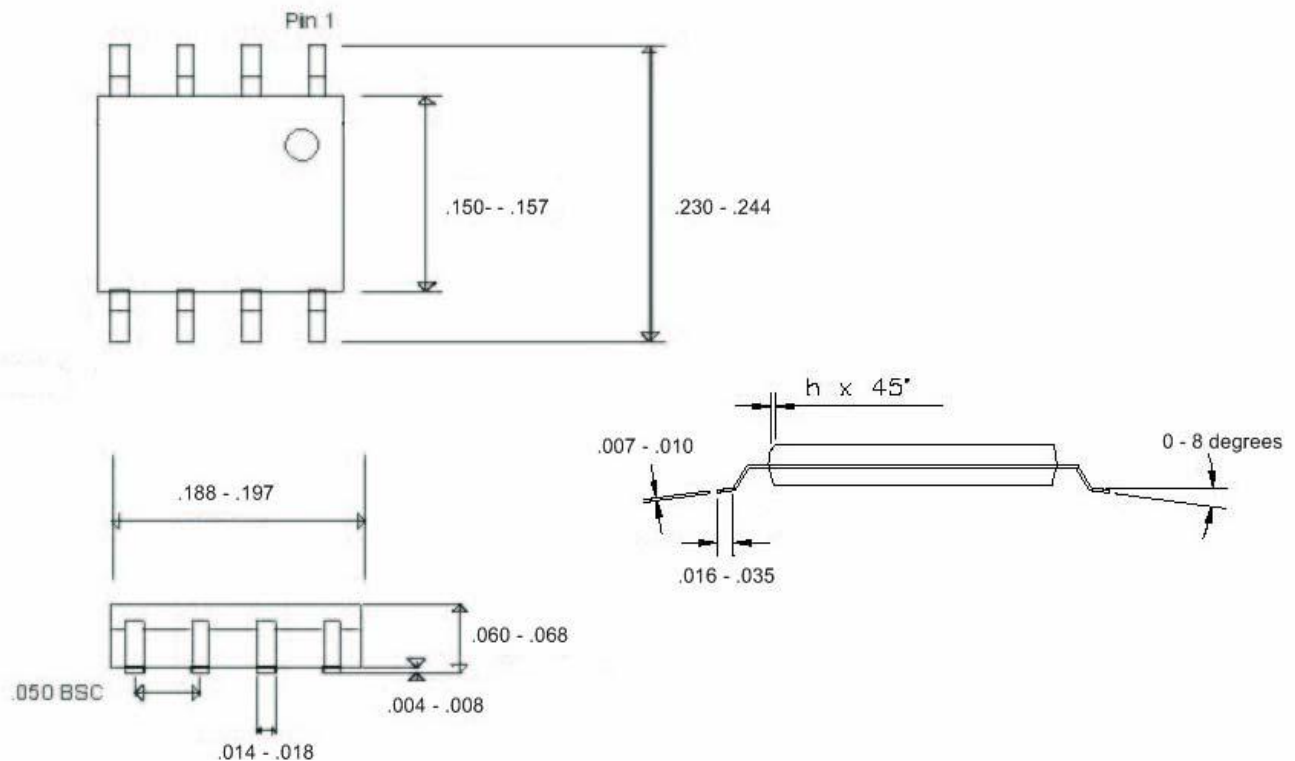


Figure 7 Mechanical Outline, 8L NB SOIC G – Green Package

## PROCESS FLOW

**Table 7 Process Flow**

PROCESS STEP	PLASTIC STANDARD	PLASTIC BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125°C	100% @ +85 or +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C
NOTES:		
1. Burn-in conditions: 125°C, 96 hrs, Vcc = 5.0V Inputs = 0V, Outputs open.		

## ORDERING INFORMATION

**Table 8 Ordering Information**

DEI PN	PART MARKING (1)	TEMPERATURE RANGE	BURN-IN	PACKAGE TYPE
DEI1041-SES-G	DEI1041 YYWWE4 SES	-55/+85 °C	NO	8L NB SOIC G
DEI1041-SMS-G	DEI1041 YYWWE4 SMS	DEI1041 YYWWE4 SES	NO	8L NB SOIC G
DEI1041-SMB-G	DEI1041 YYWWE4 SMB	-55/+125 °C	YES	8L NB SOIC G

NOTES:

1. Lot code marked on bottom. "E4" after Date Code denotes Pb Free category.

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