

# DEI1026A

## Six Channel

### Discrete-to-Digital Interface

### Sensing Open/Ground Signals

#### Features

- Senses six Open/Ground Inputs
- Inputs are lightning protected to DO-160G Level 3
- ABD0100 compliant input voltage threshold
- TTL/CMOS-Compatible Tri-State Outputs
- Package / Temperature Options:
  - 16 lead .150" SOIC, -55 °C /+85 °C or 125 °C
  - 16 lead Ceramic 300 mil SOP, -55 °C /+125 °C



SOIC package option shown

#### Functional Description

The DEI1026A is a six channel discrete-to-digital interface BiCMOS device. It senses six Open/Ground discrete signals of the type commonly found in avionic systems. The inverted 3-state outputs are TTL/CMOS compatible and are enabled by the OE and CE pins. The inputs are lightning protected to meet the requirements of DO160D Sec 22 Waveforms 3, 4, and 5, Level 3. See figures 5-7. The device is available in a 16 lead .150" SOIC and .300" Ceramic SOP.

With its reliability, low cost, operating range, and lightning protection, the DEI1026 meets a large variety of interface requirements for aerospace applications.

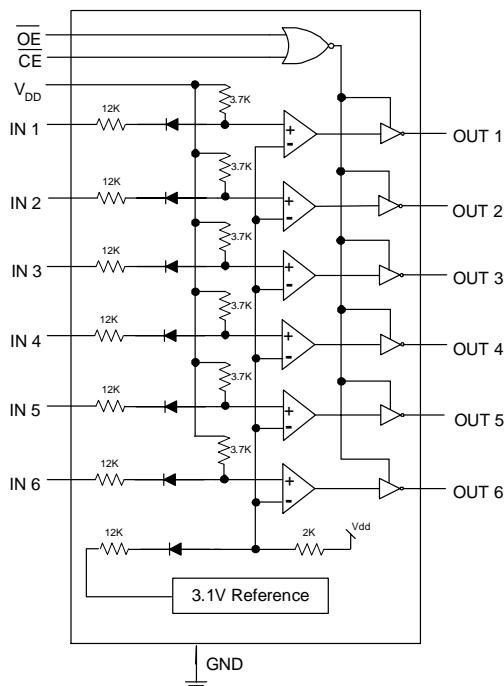


Figure 1: Concept Drawing

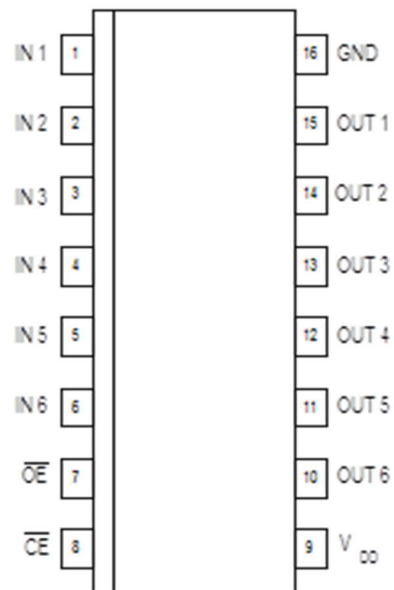


Figure 2: Pinout Diagram

## Electrical Characteristics

**Table 1: Absolute Maximum Ratings**

PARAMETER	MIN	MAX	UNITS	
Supply Voltage $V_{DD}$	-0.3	7.0	V	
Discrete Input Voltage (Pins 1-6)	-5	+40 *	V	
Digital Input Voltage ( $\overline{CE}$ and $\overline{OE}$ )	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V	
Lightning Protection (Pins 1-6) DO160G, Waveform 3; Level 3 pin injection DO160G, Waveforms 4, and 5; Level 3 pin injection	-660 -330	+660 +330	V	
Junction Temperature		145	°C	
Storage Temperature	Plastic Ceramic	-65 -55	150 150	°C
Operating Free Air Temperature	Plastic Ceramic	-55 -55	85 125	°C
Peak Body Temperature	Plastic, G Package Ceramic		260 240	°C
The DE11026A contains circuitry to protect inputs from damage due to electrostatic discharge. It has been characterized per JESD22-A114 Human Body Model to Class 1C. Observe precautions for handling and storing Electrostatic Sensitive Devices.				
* The DE11026A will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A.				

**Table 2: DE11026A Device Operating Characteristics**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$		4.5	5.0	5.5	V
Free Air Operating Temp.	$T_A$	$V_{DD} = 4.5 - 5.5$ V Plastic Ceramic	-55 -55		85 125	°C
Logic Output Sink Current	$I_{OL}$	$V_{DD} = 4.5 - 5.5$ V			5.0	mA
Logic Output Source Current	$I_{OH}$	$V_{DD} = 4.5 - 5.5$ V	-5.0			mA

**Table 3: DE11026A Logic Truth Table**

$\overline{CE}$ Chip Enable	$\overline{OE}$ Output Enable	$IN_N$ Discrete Input	$OUT_N$ Output
0	0	Open	0
0	0	Ground	1
1	X	X	High Z
X	1	X	High Z

**Table 4A: DEI1026A-SEx Electrical Characteristics**  
 (T<sub>A</sub> = -55°C to +85°C, V<sub>DD</sub> = 4.5 to 5.5 V, Unless otherwise noted)

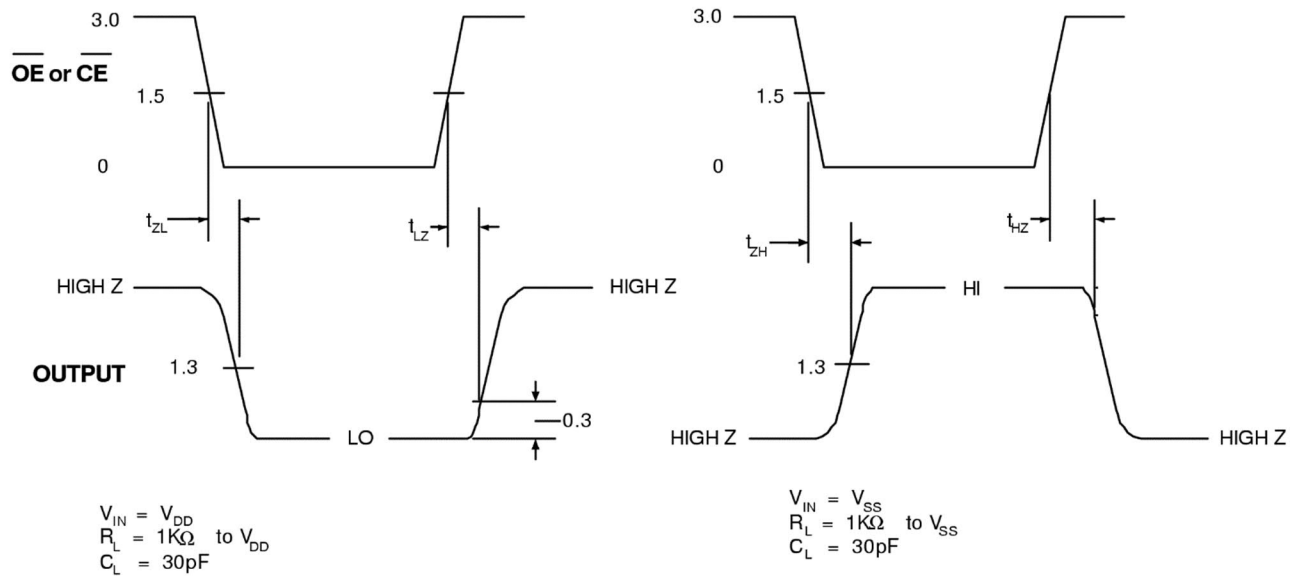
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply Characteristics</b>						
Supply Current	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>DD</sub> (all inputs) V <sub>DD</sub> = 5.5 V		5	10	mA
<b>Discrete Input Characteristics</b>						
Ground state input voltage	V <sub>SG</sub>	Voltage source from input terminal to ground for Logic High Output.			3.5	V
Open state input voltage	V <sub>SO</sub>	Voltage source from input terminal to ground for Logic Low Output.	4.1			V
Ground state input resistor	R <sub>IG</sub>	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R <sub>IO</sub>	Resistor from input to ground to guarantee Logic Low Output.	500k			Ω
Input source current	I <sub>IO</sub>	Current sourced into 100 Ohm resistor to Ground.	-100	-330		μA
Reverse leakage current	I <sub>IR</sub>	V <sub>IN</sub> = 35 V, V <sub>DD</sub> = 0 V			100	μA
<b>Logic Input Characteristics</b>						
$\overline{\text{CE}}, \overline{\text{OE}}$ input logic 1 level	V <sub>IH</sub>		2.0			V
$\overline{\text{CE}}, \overline{\text{OE}}$ input logic 0 level	V <sub>IL</sub>				0.8	V
<b>DC Output Characteristics</b>						
Output logic 1 level (TTL)	V <sub>OH</sub>	I <sub>OH</sub> = -5 mA	2.4			V
Output logic 0 level (TTL)	V <sub>OL</sub>	I <sub>OL</sub> = 5 mA (2)			0.4	V
Output logic 1 level (CMOS)	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 50mV			V
Output logic 0 level (CMOS)	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA			V <sub>SS</sub> + 50mV	V
Off-state Output Current	I <sub>OZ</sub>	$\overline{\text{OE}} = V_{DD}$ V <sub>DD</sub> = 5.5 V V <sub>OUT</sub> = 0 or V <sub>DD</sub>			+/-10	μA
<b>Switching Characteristics [1]</b>						
I/O propagation delay	t <sub>HL</sub> , t <sub>LH</sub>	Refer to Figure 4.			150	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output low) to output HI-Z	t <sub>LZ</sub>	Refer to Figure 3.			25	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output HI-Z) to output low	t <sub>ZL</sub>	Refer to Figure 3.			25	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output high) to output HI-Z	t <sub>HZ</sub>	Refer to Figure 3.			25	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output HI-Z) to output high	t <sub>ZH</sub>	Refer to Figure 3.			25	ns

**Table 4B: DE11026A-xMx Electrical Characteristics**  
 (T<sub>A</sub> = -55°C to +125°C, V<sub>DD</sub> = 4.5 to 5.5 V, Unless otherwise noted)

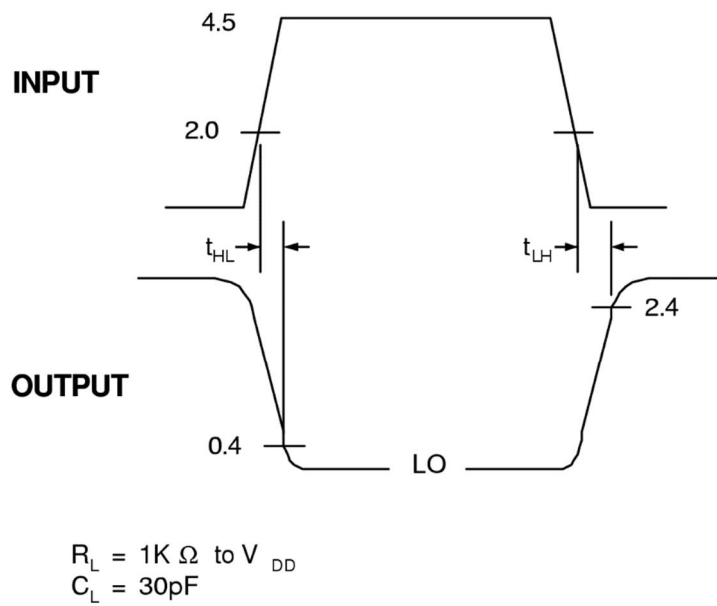
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply Characteristics</b>						
Supply Current	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>DD</sub> (all inputs) V <sub>DD</sub> = 5.5 V		5	10	mA
<b>Discrete Input Characteristics</b>						
Ground state input voltage	V <sub>SG</sub>	Voltage source from input terminal to ground for Logic High Output.			3.5	V
Open state input voltage	V <sub>SO</sub>	Voltage source from input terminal to ground for Logic Low Output.	4.1			V
Ground state input resistor	R <sub>IG</sub>	Resistor from input to ground to guarantee Logic High Output.	0		100	Ω
Open state input resistor	R <sub>IO</sub>	Resistor from input to ground to guarantee Logic Low Output.	500k			Ω
Input source current	I <sub>IO</sub>	Current sourced into 100 Ohm resistor to Ground.	-100	-330		μA
Reverse leakage current	I <sub>IR</sub>	V <sub>IN</sub> = 35 V, V <sub>DD</sub> = 0 V			100	μA
<b>Logic Input Characteristics</b>						
$\overline{\text{CE}}$ , $\overline{\text{OE}}$ input logic 1 level	V <sub>IH</sub>		2.0			V
$\overline{\text{CE}}$ , $\overline{\text{OE}}$ input logic 0 level	V <sub>IL</sub>				0.8	V
<b>DC Output Characteristics</b>						
Output logic 1 level (TTL)	V <sub>OH</sub>	I <sub>OH</sub> = -5 mA	2.4			V
Output logic 0 level (TTL)	V <sub>OL</sub>	I <sub>OL</sub> = 5 mA (2)			0.4	V
Output logic 1 level (CMOS)	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 50mV			V
Output logic 0 level (CMOS)	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA			V <sub>SS</sub> + 50mV	V
Off-state Output Current	I <sub>OZ</sub>	$\overline{\text{OE}} = V_{DD}$ V <sub>DD</sub> = 5.5 V V <sub>OUT</sub> = 0 or V <sub>DD</sub>			+/-10	μA
<b>Switching Characteristics [1]</b>						
I/O propagation delay	t <sub>HL</sub> , t <sub>LH</sub>	Refer to Figure 4.			170	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output low) to output HI-Z	t <sub>LZ</sub>	Refer to Figure 3.			30	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output HI-Z) to output low	t <sub>ZL</sub>	Refer to Figure 3.			30	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output high) to output HI-Z	t <sub>HZ</sub>	Refer to Figure 3.			30	ns
Delay from $\overline{\text{CE}}$ or $\overline{\text{OE}}$ input (with output HI-Z) to output high	t <sub>ZH</sub>	Refer to Figure 3.			30	ns

Notes:

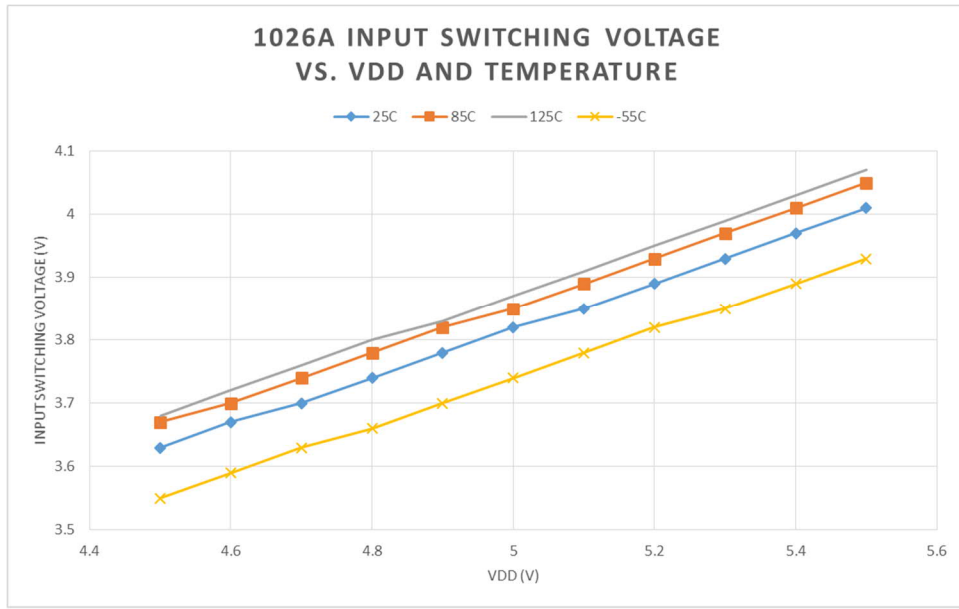
1. Guaranteed by design and not production tested.
2. Limit the sum of all IOL currents to 20 ma. The Vsg spec may exceed limit beyond this current.



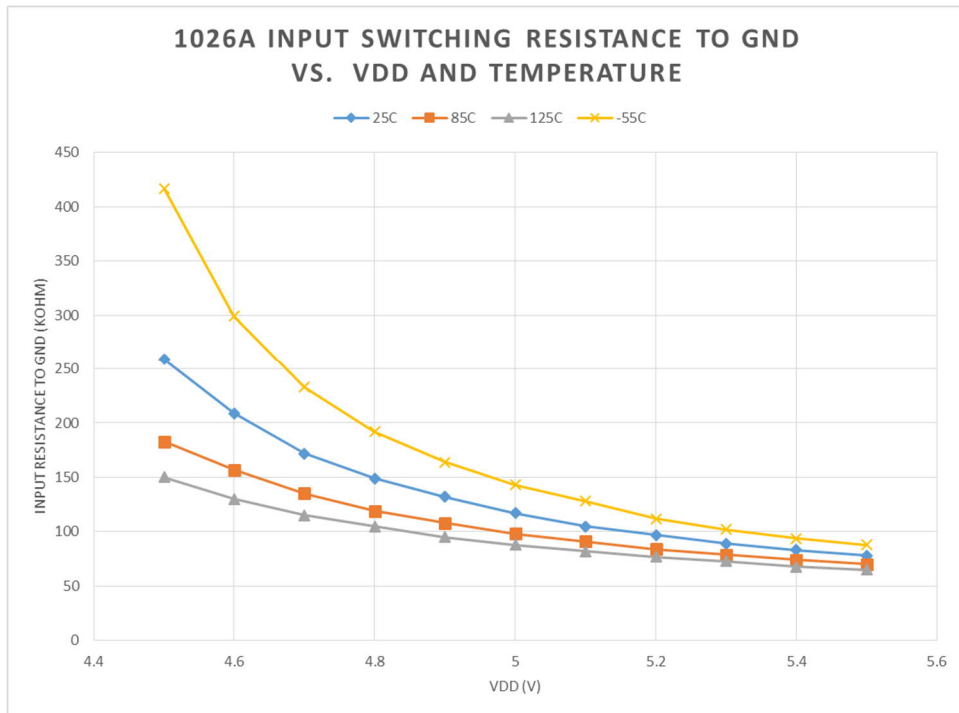
**Figure 3: Enable to Output Propagation Delay**



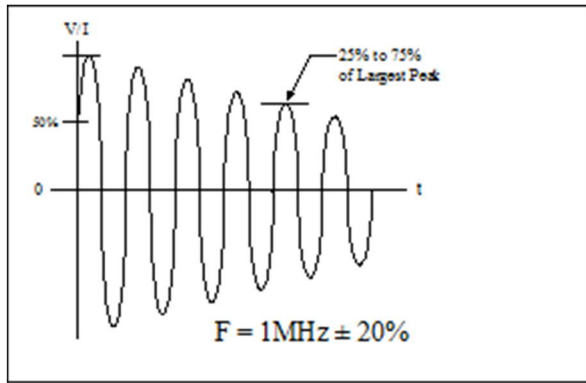
**Figure 4: Input to Output Propagation Delay**



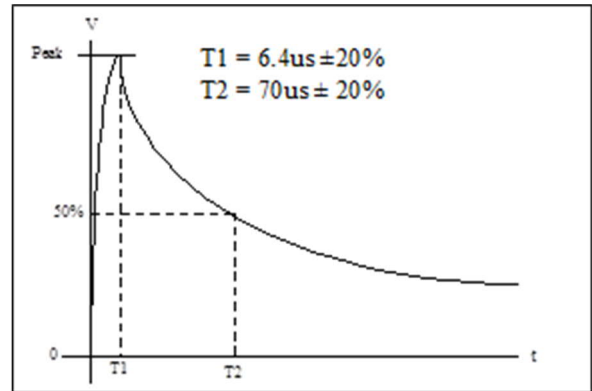
**Figure 5 Input Switching Threshold Voltage Characteristics**



**Figure 6 Input Switching Resistance to Ground Characteristics**



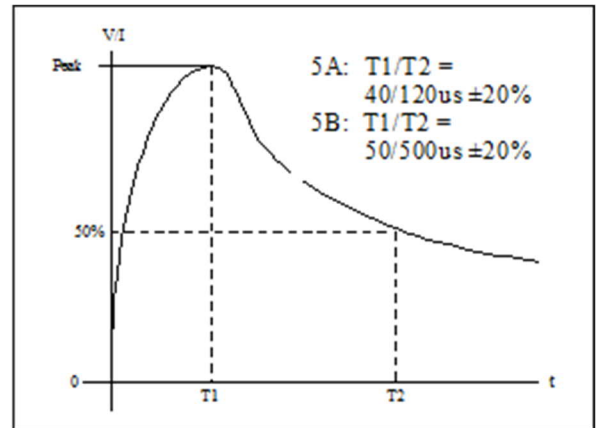
DO160 WF3 Voc/Isc Waveform



DO160 WF4 Voc/Isc Waveform

Notes:

1. DO160G pin injection Level 3 waveforms.
2. Voltage tolerance: +20%, -0%
3. Waveform Source Impedance characteristics:
  - Waveform 3 Voc/Isc = 600 V / 24 A => 25 Ω
  - Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ω
  - Waveform 5A Voc / Isc = 300V / 300A => 1 Ω



DO160 WF5 Voc/Isc Waveform

Figure 7 DO160G Pin Injection Test Waveforms

## Package Characteristics

Table 5: Package Characteristics		
PACKAGE TYPE	16 Lead SOIC Narrow Body, Green	16 Lead Ceramic SOP
REFERENCE	16L SOIC NB G	16L CSOP
<b>THERMAL RESISTANCE:</b>		
$\theta_{JA}$ (4 layer PCB with Power Planes)	~74 °C/W	-
$\theta_{JC}$	~30 °C/W	23 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C	Hermetic
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4	Au e4
Pb-Free DESIGNATION	RoHS Compliant	Pb Free
JEDEC REFERENCE	MS-012-AC	-

16L SOIC NB G

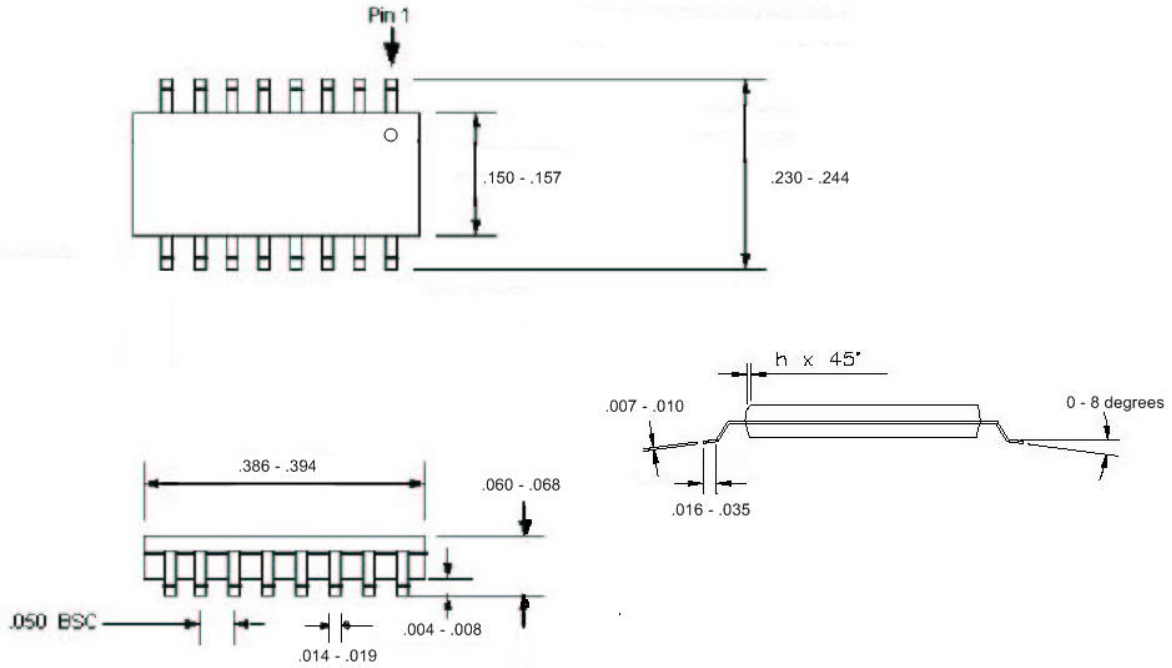


Figure 8: 16L SOIC Mechanical Outline

16L CSOP

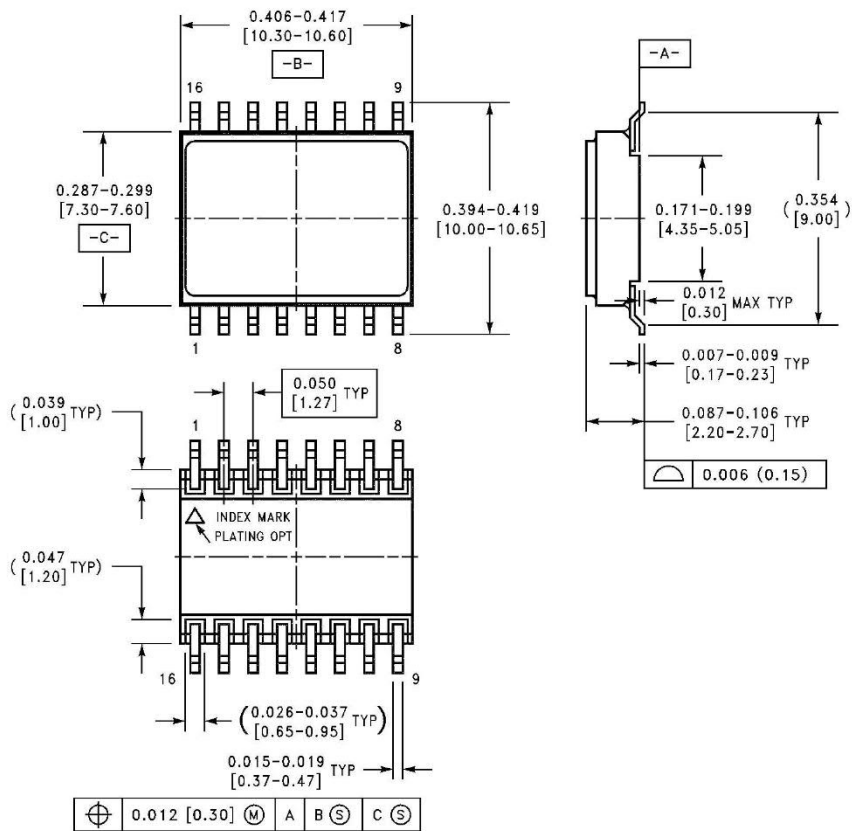


Figure 9: 16L CSOP Mechanical Outline



## Ordering Information

<b>Table 6: Ordering Information</b>				
<b>DEI PART NUMBER</b>	<b>MARKING (1)</b>	<b>PACKAGE</b>	<b>OP. TEMP. RANGE</b>	<b>PROCESSING</b>
DEI1026A-SES-G	DEI1026A-SES E4	16L SOIC NB G	-55 / +85 °C	Standard
DEI1026A-SMS-G	DEI1026A-SMS E4 (3)	16L SOIC NB G	-55 / +125 °C	Standard
DEI1026A-WMS	DEI1026A-WMS	16 lead ceramic SOP	-55 / +125 °C	Standard
DEI1026A-WMB	DEI1026A-WMB	16 lead ceramic SOP	-55 / +125 °C	Burn In, 96 hr @ 125 °C
<b>NOTES:</b> 1. All packages marked with Lot Code and Date Code. 2. "E4" after Date Code Denotes Pb Free category. 3. Alternate marking is –SES + Blue Dot				

DEI reserves the right to make changes to any products or specifications herein. DEI makes no warranty, representation, or guarantee regarding suitability of its products for any particular purpose.