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DEI1049 OCTAL ARINC 429 LINE RECEIVER

FEATURES

- Octal ARINC 429 to TTL/CMOS logic line receivers
- Operates from single +5 V \pm 10% or 3.3 V \pm 10% power supply
- Operates in high noise environment
 - Input Common Voltage Range: \pm 20 V
 - 2 V minimum Input hysteresis
- DEI1049 operates with external 40 k Ω resistors on inputs
 - Lightning protection beyond Level 3
 - Fault isolation
- Package: 38L TSSOP, 4.4 mm body
- Withstands inadvertent short to 115 Vac on inputs

DEI1049 PINOUT

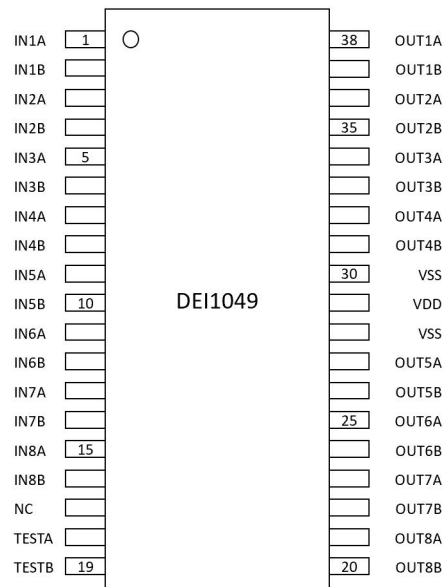


Table 1 DEI1049 Pin Description

PIN	NAME	DESCRIPTION
15, 13, 11, 9, 7, 5, 3, 1	IN[8:1]A	429 INPUTS. ARINC 429 format serial digital data "A" inputs.
16, 14, 12, 10, 8, 6, 4, 2	IN[8:1]B	429 INPUTS. ARINC 429 format serial digital data "B" inputs.
17	NC	Reserved pin for DEI use only
18	TESTA	LOGIC INPUT, Test input A
19	TESTB	LOGIC INPUT, Test input B
21, 23, 25, 27, 32, 34, 36, 38	OUT[8:1]A	LOGIC OUTPUTS. CMOS/TTL format serial digital data "A" outputs.
20, 22, 24, 26, 31, 33, 35, 37	OUT[8:1]B	LOGIC OUTPUTS. CMOS/TTL format serial digital data "B" outputs.
29	VDD	POWER INPUT. 5 VDC or 3.3 VDC.
28, 30	VSS	POWER INPUT. Ground.

FUNCTIONAL DESCRIPTION

The DEI1049 is a BiCMOS device which contains eight differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. Each channel operates independently and meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to

Figure 1 DEI1049 Block Diagram and Truth Table.

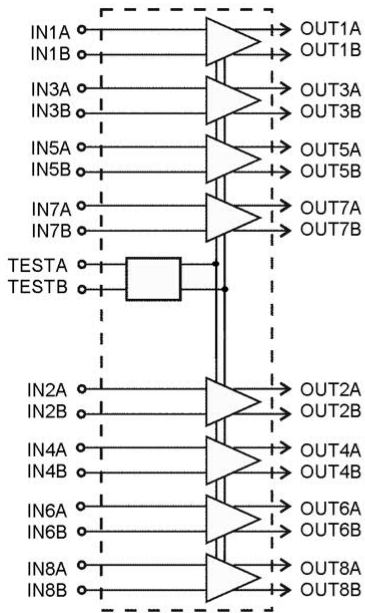
The device is designed to operate in a high noise environment. Inputs are accepted over a \pm 20 V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

The DE11049 device provides logic level TEST inputs for built in system test. They force the outputs of all eight receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode. The DE11049 has a single test port which controls all 8 channels.

The DE11049 is equivalent to the DE11046A product, but with 40 kΩ of the input resistors removed so the part will operate with external 40 kΩ resistors. The DE11049 ARINC inputs must be connected to the ARINC bus through 40 kΩ series resistors for correct operation. The external resistors provide fault isolation in the event of IC damage that might otherwise cause excessive loading of the ARINC signals.

The ARINC inputs incorporate on-chip lightning protection by use of high value resistors on the inputs to minimize IR heating. The resistors have dielectric isolation to withstand the voltage transients. The inputs withstand lightning induced transients up to and including DO160 Level 3 pin injection levels. Higher levels can be achieved with the addition of external transient voltage suppressor (TVS) devices between the inputs and ground. The 40 kΩ resistors limit surge current and thus minimize the power requirement and size of the TVS.

The ARINC inputs withstand inadvertent short to 115 Vac aircraft power without sustaining damage.



INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TESTA	TESTB	INA - INB	OUTA	OUTB	Logic
0	0	Logic +1	1	0	ONE
0	0	Logic -1	0	1	ZERO
0	0	NULL	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL

Figure 1 DE11049 Block Diagram and Truth Table

ELECTRICAL DESCRIPTION

Table 2: Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to VSS)	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)		115	Vac
Power Dissipation @ 85 °C		800	mW
Junction Temperature, Tjmax (limited by molding compound Tg)		145	°C
Peak Body Temperature		260	°C
Lightning Protection (ARINC 429 Channel Inputs) Waveform 3 (2) Waveform 4, & 5A (2) (3)	-720 -360	+720 +360	V V
ESD JS-001-2017 HBM		1B	Class
Notes: 1. Stresses above these limits can cause permanent damage. 2. Per DO160, Sect 22 Level 3 pin injection. See Figures 4, 5 and 6. 3. Inputs can be protected to withstand higher stress by adding shunt TVS on inputs. Inputs withstand 1500 V Waveform 5A when clipped \leq 600 V.			

Table 3: Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	+5 V \pm 10% +3.3 V \pm 10%
Logic Input Levels	TESTA, B	0 to VDD
Operating Temperature -TES -TMS		-55 to +85 °C -55 to +125 °C

Table 4: Electrical Characteristics

Conditions: Temperature: -55 °C to +85 °C (-TES); -55 °C to +125 °C (-TMS) VDD = +5 V ±10% or 3.3 V ±10% INA/B inputs have 40 kΩ resistors installed between the IC pins and A429 signal.					
PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNITS
ARINC INPUTS					
$V_A - V_B = \text{Logic } +1$	OUTA = 1	V_{+1}	6.5	13	V
$V_A - V_B = \text{Logic } -1$	OUTB = 1	V_{-1}	-6.5	-13	V
$V_A - V_B = \text{Logic Null}$	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	2.5	V
Input Hysteresis		V_{HY}	2.0	4.0	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20	+20	V
Input Resistance IN_A to IN_B	VDD open, Shorted to VSS or +5 V (1)	R_{IN}	280		kΩ
Input Resistance IN_A or IN_B to V_{SS}	VDD open, Shorted to VSS or +5 V	R_s	140		kΩ
Input Capacitance IN_A to IN_B	VDD open, Shorted to VSS or +5 V (1)	C_{IN}		10	pF
Input Capacitance IN_A or IN_B to V_{SS}	VDD open, Shorted to VSS or +5 V (1)	C_s		10	pF
LOGIC INPUTS					
Logic 0 Voltage		V_{IL}		0.8	V
Logic 1 Voltage		V_{IH}	2.0		V
Logic 0 Current	$V_{\text{IL}} = 0.8$	I_{IL}		25	μA
Logic 1 Current	$V_{\text{IH}} = 2.0$	I_{IH}		50	μA
LOGIC OUTPUTS					
OUTPUT HIGH VOLTAGE TTL	$I_{\text{OH}} = -5 \text{ mA}$ (VDD = 5.0 V) $I_{\text{OH}} = -5 \text{ mA}$ (VDD = 3.3 V) TTL Compatible	V_{OH}	2.4		V
OUTPUT LOW VOLTAGE TTL	$I_{\text{OL}} = 5 \text{ mA}$ (VDD = 5.0 V)	V_{OL}		0.4	V
OUTPUT HIGH VOLTAGE CMOS	$I_{\text{OH}} = 100 \text{ μA}$ CMOS Compatible	V_{OH}	$V_{\text{DD}} - 50 \text{ mV}$		V
OUTPUT LOW VOLTAGE CMOS	$I_{\text{OL}} = 100 \text{ μA}$ CMOS Compatible	V_{OL}		$V_{\text{SS}} + 50 \text{ mV}$	V
SUPPLY CURRENT					
VDD Current	Data Rate = 0 MHZ, $IN_A/B = \text{open}$, $OUTA/B = \text{open}$, VDD = 5.5 V or 3.63 V	I_{DD}	1.5	8.5	mA
Notes: 1. Guaranteed by design, not production tested. 2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to VSS unless otherwise noted.					

Table 5: Switching Characteristics

PARAMETER	TEST CONDITION (1, 2)	SYMBOL	MAX VDD 3.3 V	MAX VDD 5 V	UNITS
INA/B to OUTA/B Prop Delay	TESTA = TESTB = 0 C _L = 50 pF	t _{LH}	1000	900	ns
INA/B to OUTA/B Prop Delay	TESTA = TESTB = 0 C _L = 50 pF	t _{HL}	1000	900	ns
OUTA/B rise time	10% to 90%, C _L = 50 pF	t _r	50	25	ns
OUTA/B fall time	10% to 90%, C _L = 50 pF	t _f	50	25	ns
TESTA/B to OUTA/B Prop delay	C _L = 50 pF	t _{TOH}	100	60	ns
TESTA/B to OUTA/B Prop delay	C _L = 50 pF	t _{TOL}	100	60	ns

Notes:
1. Sample tested.
2. Refer to Figures 2 – 3.

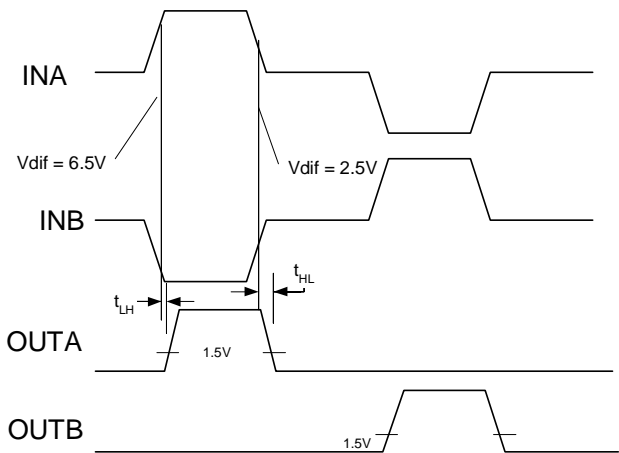


Figure 3 ARINC 429 Input to Logic Output Switching Waveform

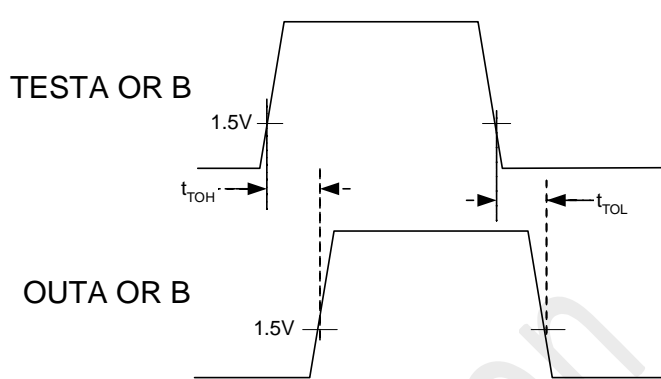


Figure 2 TEST Input to Logic Output Switching Waveform

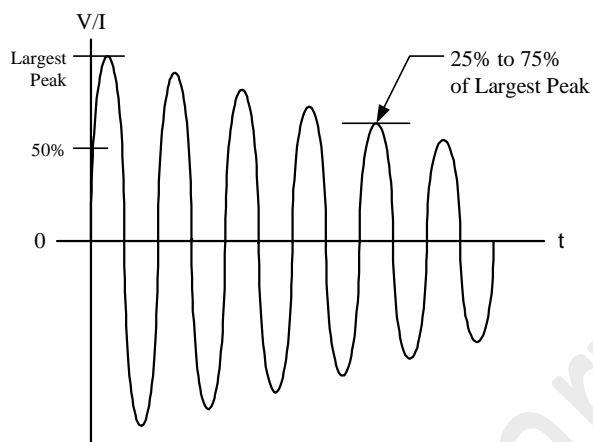


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #3.

$V_{oc} = 600 \text{ V}$, $I_{sc} = 24 \text{ A}$, Frequency = $1 \text{ MHz} \pm 20\%$

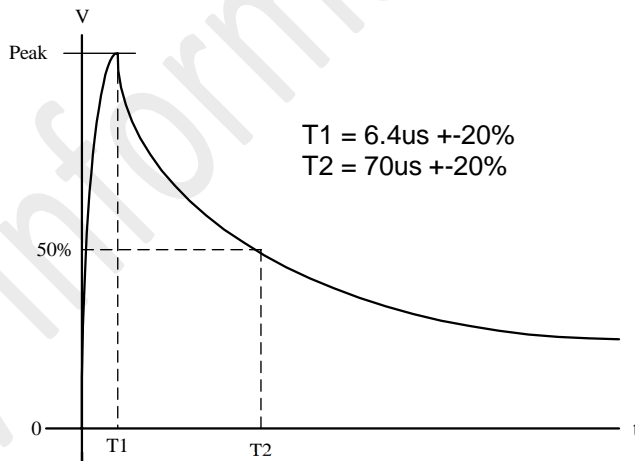


Figure 4 DO160 Lightning Induced Transient Voltage Waveform #4

$V_{oc} = 300 \text{ V}$, $I_{sc} = 60 \text{ A}$

LIGHTNING TRANSIENT NOTES:

1. V_{oc} = Peak Open Circuit Voltage available at the calibration point.
2. I_{sc} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of V_{oc} to I_{sc} is the generator source impedance to be used for generating the waveforms.

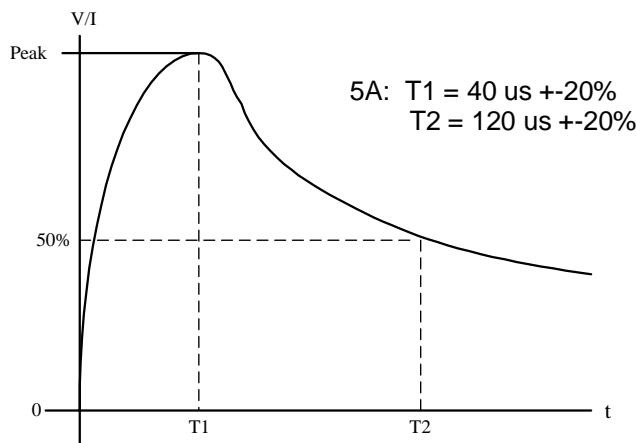


Figure 6 DO160 Lightning Induced Transient Voltage Waveform #5.

$V_{oc} = 300 \text{ V}$, $I_{sc} = 300 \text{ A}$

ORDERING INFORMATION

Table 6: Ordering Information

DEI PN	MARKING (1)	TEST INPUTS	TEMPERATURE RANGE	PACKAGE	SCREENING
DEI1049-TES-G	DEI1049-TES (e4)	YES	-55/+85 °C	38L TSSOP G	Standard
DEI1049-TMS-G	DEI1049-TMS (e4)	YES	-55/+125 °C	38L TSSOP G	Standard

Notes:

1. All packages marked with Lot Code and Date Code. (e4) after Date Code denotes Pb Free category.

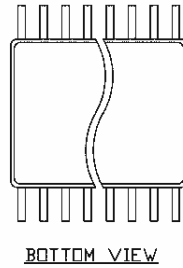
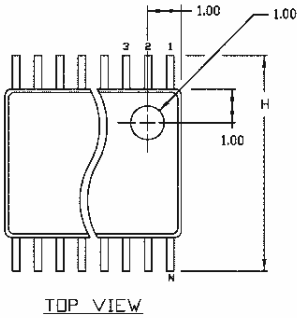
Table 7: Screening Process

SCREENING	STANDARD
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ 85 °C or 125 °C
LOW TEMPERATURE	0.65% AQL@-55 °C

PACKAGE DESCRIPTION

Table 8: Package Characteristics

CHARACTERISTIC	VALUE
REFERENCE	38L TSSOP G
Θ_{JA} (4 layer PCB with Power Planes)	75 °C/W
Θ_{JC}	15 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 2 / 260 °C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MO-153-BD-1



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.17	0.27	.0067	.0106
b ₁	0.17	0.23	.0067	.0091
c	0.090	0.200	.0035	.0079
c ₁	0.090	0.135	.0035	.0053
D	9.60	9.80	.3780	.3858
E	4.30	4.50	.169	.177
e	0.50 BSC		0.0197 BSC	
H	6.30	6.50	.248	.256
L	0.50	0.70	.020	.028
α	0°	8°	0°	8°

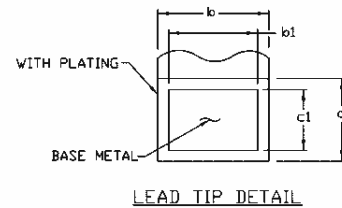
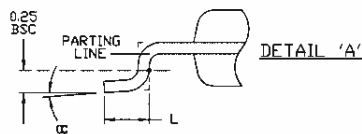
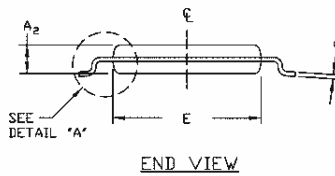
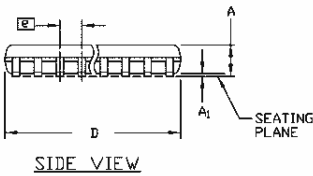


Figure 6 38L TSSOP Mechanical Outline

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