

DEI1166

OCTAL GND/OPEN INPUT, PARALLEL OUTPUT INTERFACE IC

FEATURES

- Eight GND/OPEN discrete inputs
 - Internal pull up resistor with 1mA source current to prevent dry relay contacts
 - Internal isolation diode
 - Inputs protected from Lightning Induced Transients per DO160, Section 22 Level 3 pin injection
 - Hysteresis provides noise immunity
- 3.3 V or 5 V TTL/CMOS compatible digital IO
 - 8 tri-state outputs
 - /CS & /OE control inputs
- VCC Logic Supply: 3.3 V or 5 V
- VDD Analog Supply: 5 V to 18 V
- 24L TSSOP package



PIN ASSIGNMENTS

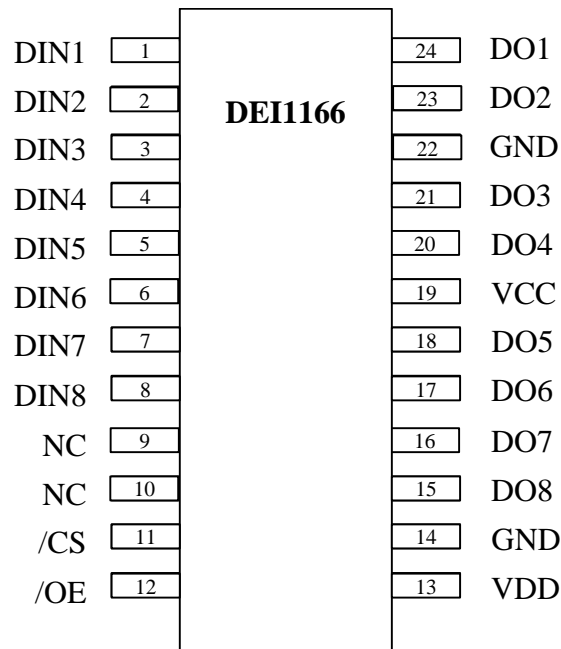


Figure 1 DEI1166 Pin Assignment

Table 1 Pin Descriptions

PIN	NAME	DESCRIPTION
8-1	DIN[8:1]	Discrete Inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The threshold and hysteresis characteristics are determined by the applied VDD voltage.
9-10	NC	Not Connected.
11	/CS	Chip Select Logic Input. Low input selects the device. Has an internal pull-up to VCC.
12	/OE	Output Enable Logic Input. Low input when /CS is low will enable the tri-state outputs. Has an internal pull-up to VCC.
13	VDD	Analog Supply. +5 to +18 V
14	GND	Analog Ground.
19	VCC	Logic Supply. +3.3 V or +5 V
22	GND	Logic Ground.
15,16,17,18,20,21,23,24	DO[8:1]	Logic Outputs. Eight tri-state data outputs.

FUNCTIONAL DESCRIPTION

The DEI1166 is an eight-channel parallel-output discrete-to-digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via a parallel 3-state output.

Table 2 Truth Table

/CE	/OE	DIN[8:1]	DO[8:1]
L	L	Open	L
L	L	Ground	H
H	X	X	High Z
X	H	X	High Z

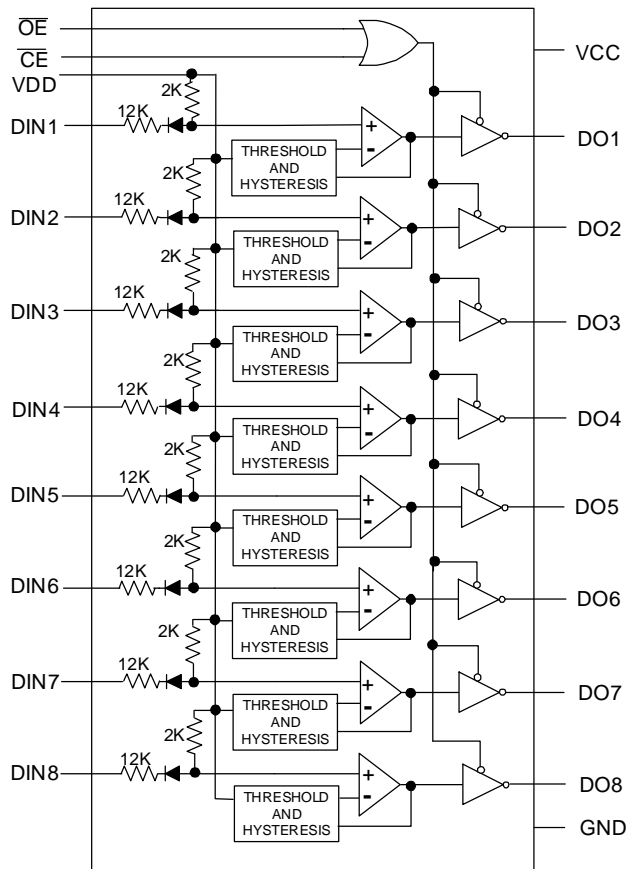


Figure 2 DEI1166 Function Diagram

DIN INPUT

The DIN inputs are converted to logic levels via input conditioning networks and comparators. The logic signals are applied to inverting tri-state output buffers. A high level on a DIN input will result in a logic '0' on its respective DO output.

Each discrete input consists of the circuit shown in Figure 3. Each DIN signal is conditioned by the resistor / diode network and presented to the comparator IN+. The comparator IN-, and therefore the switching threshold, is developed from the VDD supply voltage. It includes positive feedback from the comparator output to provide hysteresis. Some notable features are:

- The comparator includes an RC filter to provide noise rejection of transient pulses of up to several μ s. Thus, there is a relatively large DIN setup time. (Refer to timing parameter tsu2).
- The inputs can withstand continuous input voltages of 40 V minimum. The isolation diode breakdown voltage is greater than 50 V. The 12 k Ω input resistor is designed to limit diode breakdown current to safe levels during lightning transient events.

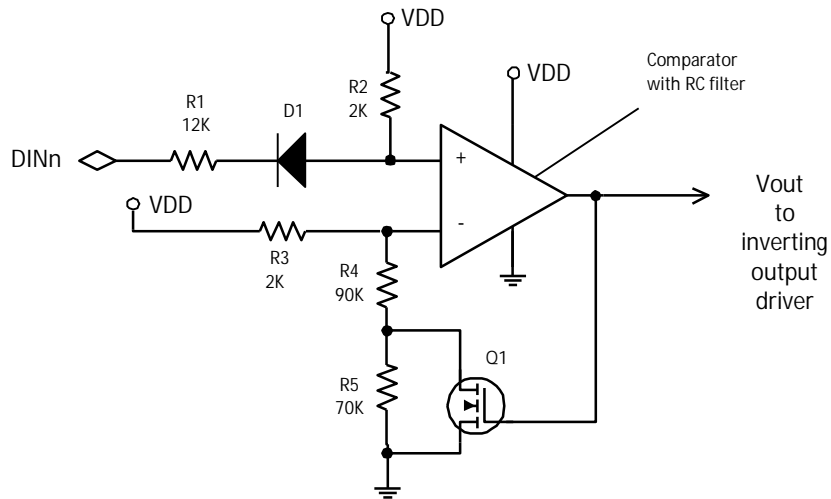


Figure 3 Discrete Input Circuit

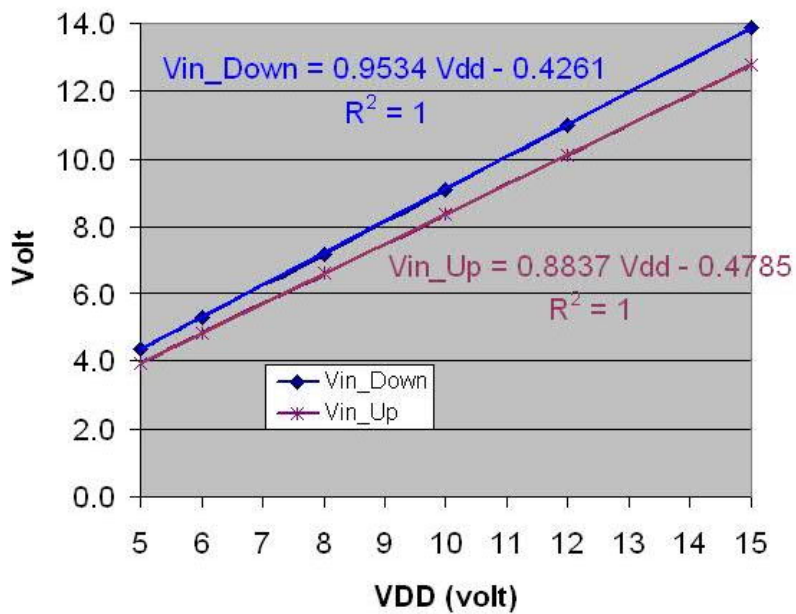


Figure 4 DIN Threshold vs. VDD

Figure 5 depicts the resistance value that when applied between the input and ground, causes the comparator to switch. Lower input switching resistance values can be achieved by adding an external diode isolated pull-up resistor to the VDD (or a higher voltage) supply.

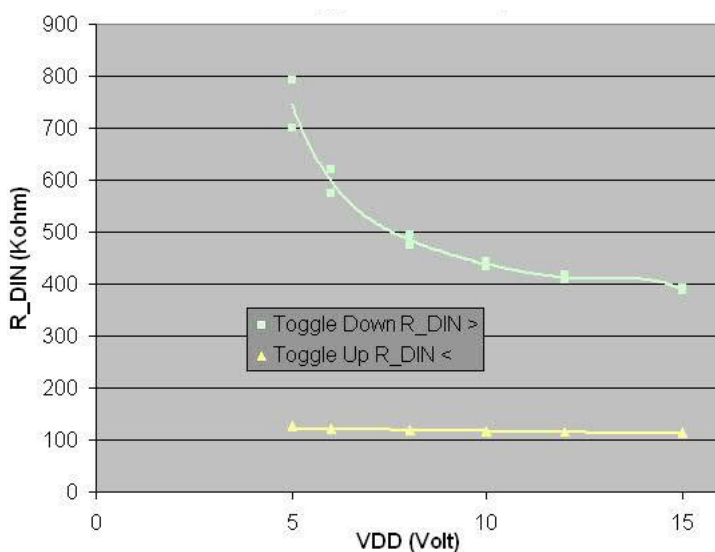


Figure 5 Input switching resistance

LIGHTNING PROTECTION

DIN inputs are designed to survive lightning induced transients as defined by RTCA DO160 Section 22 Level 3 pin injection Waveforms 3, 4, and 5A.

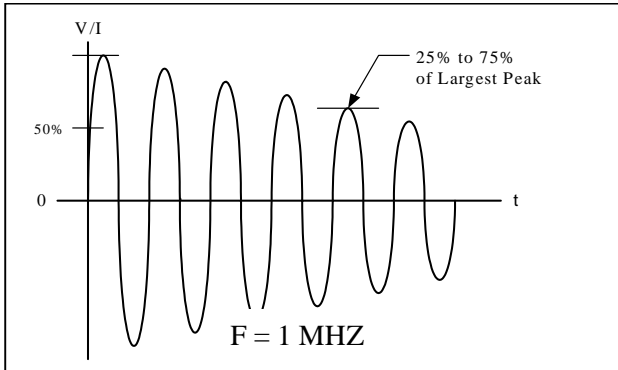


Figure 6 Voltage / Current Waveform 3

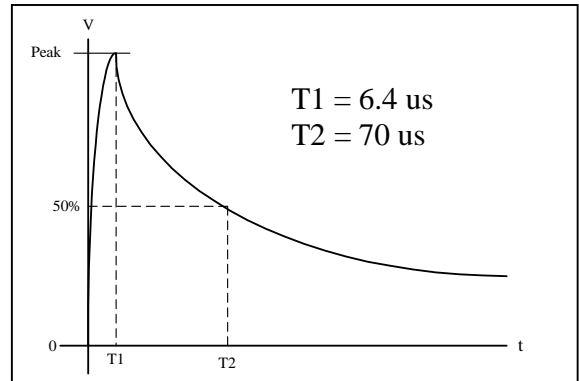


Figure 7 Voltage / Current Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600 V / 24 A => 25 Ω
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ω
- Waveform 5A Voc / Isc = 300 V / 300 A => 1 Ω

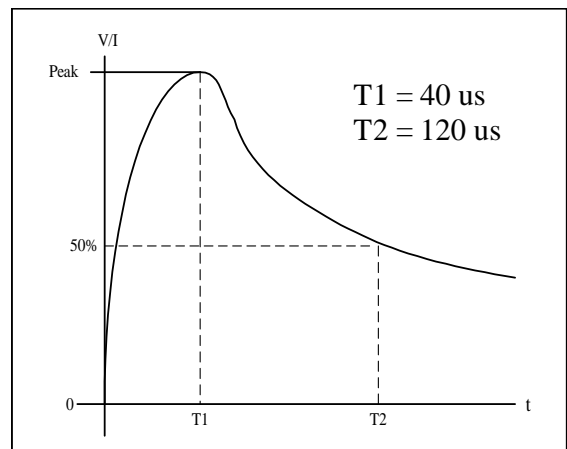


Figure 8 Voltage / Current Waveform 5A

NOTE

It is possible to achieve higher level lightning immunity by adding a 1 k Ω series resistor and a Transient Voltage Suppressor (TVS) to clamp the inputs below 600 V. The 1 k Ω resistance reduces the input threshold. For example, with VDD = 15 V, the thresholds become:

Max LH threshold = 15.3 V
 Min HL threshold = 11.3 V

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
VCC Supply Voltage	-0.3	+7.0	V
VDD Supply Voltage	-0.3	20	V
Operating Temperature Plastic Package	-55	+125	°C
Storage Temperature Plastic Package	-65	+150	°C
Input Voltage			
DIN[8:1] Continuous	-5	+40	V
DO160, Waveform 3, Level 3	-600	+600	V
DO160, Waveform 4 and 5, Level 3	-300	+300	V
Logic Inputs	-1.5	VCC + 1.5	V
DO[8:1]	-0.5	VCC + 0.5	V
Power Dissipation @ 85 °C: (> 10 Sec) 24L TSSOP		0.8	W
Junction Temperature: Tjmax, Plastic Packages		145	°C
ESD per JEDEC A114-A Human Body Model			
Logic and Supply pins		2000	V
DIN pins		1000	
Peak Body Temperature		260	°C
Notes:			
1. Voltages referenced to Ground			
2. Stresses above absolute maximum ratings may cause permanent damage to the device.			

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC	5.0 V ±10%, 3.3 V ±10%
	VDD	5.0 to 18 V
Logic Inputs	/CS, /OE	0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40 V
Operating Temperature		
-TES		-55 to +85 °C
-TMS		-55 to +125 °C

Table 5 DC Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
LOGIC INPUTS AND OUTPUTS					
V _{IH}	High level input voltage		2.0		V
V _{IL}	Low level input voltage			0.8	V
V _{OH}	High level output voltage	I _{OUT} = -20 uA	VCC – 0.1		V
		VCC = 5 V ±10% I _{OUT} = -4.5 mA	3.0		V
V _{OL}	Low level output voltage	I _{OUT} = 20 uA		0.1	V
		VCC = 5 V ±10% I _{OUT} = 4.5 mA		0.40	V
I _{oz}	Output 3-state leakage current	Output in Hi Impedance state. Vout = 0 V to 5 V		±10	uA
I _{IL}	Low level input current	VIN = 0 V	-50	-300	uA
Cin	Input Capacitance.			10	pF
Cout	DO pin capacitance	Output in Hi-Z state.		15	pF
DISCRETE INPUTS VDD = +14 V					
V _{IH}	High level input voltage	-55/+85 °C -55/+125 °C	13.3 13.5		V
V _{IL}	Low level input voltage			11.5	V
V _{Ihst}	Input hysteresis voltage		0.9		V
I _{IH}	High level input current	Vin = 18 V Vin = 40 V		10 40	uA
I _{IL}	Low level input current	Vin = 0 V	-0.7	-1.3	mA
DISCRETE INPUTS VDD = +5.0 V					
V _{IH}	High level input voltage	-55/+85 °C -55/+125 °C	4.7 4.8		V
V _{IL}	Low level input voltage			3.5	V
V _{Ihst}	input hysteresis voltage		0.35		V
I _{IH}	High level input current	Vin = 18 V Vin = 40 V	1	10 40	uA
I _{IL}	Low level input current	Vin = 0 V	-0.21	-0.43	mA
SUPPLY CURRENT (VCC = 5.5 V, VDD = +14 V)					
ICC	Max quiescent logic supply current	Vin(logic) = VCC or GND DIN[8:1] = open		400	uA
IDD	Max quiescent analog supply current	Vin(logic) = VCC or GND DIN[8:1] = Open		11.5	mA
		DIN[8:1] = GND		24	

Notes:

- Conditions (unless otherwise stated): VCC = 5.0 V ±10% or 3.3 V ±10%, VDD = 5.0 to 18 V. Temperature = rated temperature range.
- Voltages referenced to Ground. Currents into device are positive, currents out of device are negative.

Table 6 AC Electrical Characteristics

SYMBOL	PARAMETER (VDD=+5.0V)	VCC (V)	LIMITS		UNIT
			-55 to +85 °C	-55 to +125 °C	
tZLmax	Maximum propagation delay, /CS↓ and /OE↓ to DO low. (1) (3)	3.0 4.5 5.5	100 53 42	113 59 46	ns
tZHmax	Maximum propagation delay, /CS↓ and /OE↓ to DO high (1) (3)	3.0 4.5 5.5	100 53 42	113 59 46	ns
tHZmax	Maximum propagation delay, /CS↑ or / OE↑ to DO HI-Z. from DO Low or high. (1) (2) (3)	3.0 4.5 5.5	100 71 65	110 78 72	ns
tHLmin tLHmin	Minimum data propagation delay, DIN to DO (4) (5)	5.0	3.5	3.5	us
tHLmax tLHmax	Maximum data propagation delay, DIN to DO (4) (5)	5.0	420	630	us

Notes:

1. DO is loaded with 30 pF to GND.
2. DO is loaded with 10 kΩ to GND for High output, 10 kΩ to VCC for Low output.
3. Timing measured from VIN = 1.5 V to VOU T = 200 mV. See Figure .
4. See Figure 10. The delay is due to both the on-chip filter circuits and VDD.
5. Guaranteed by design.
6. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to GND.

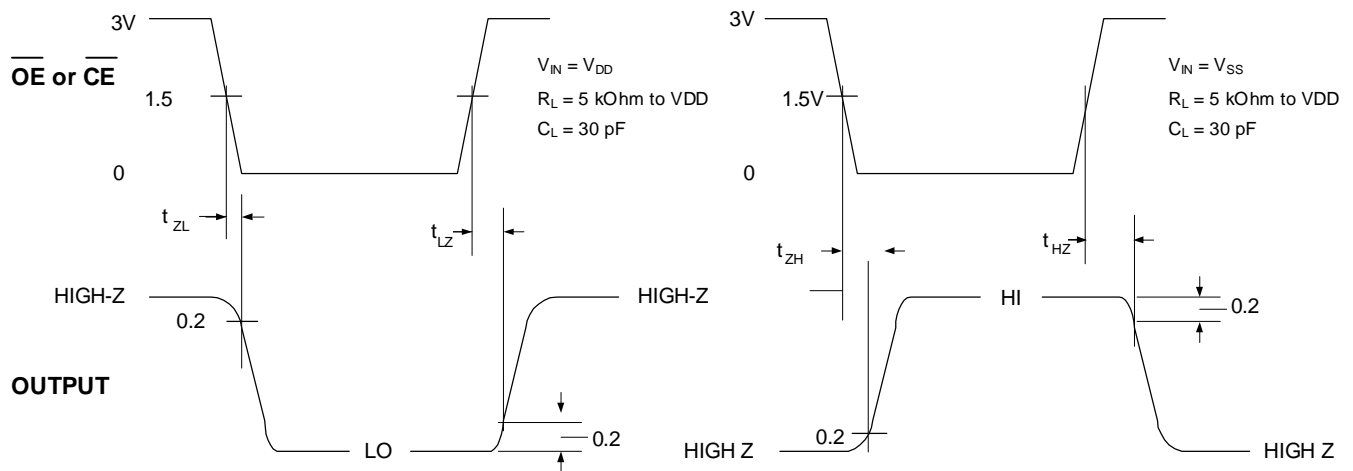


Figure 9 Chip Select or Output Enable to Output Delay

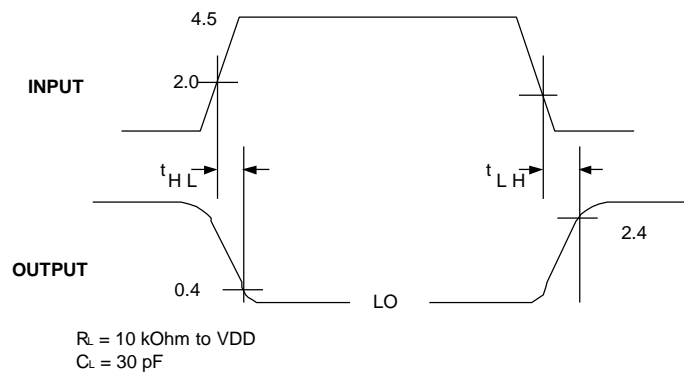


Figure 10 Input to Output Delay

PACKAGE DESCRIPTION

24L TSSOP

Moisture Sensitivity:	MSL 1 / 260 °C
Θ _{ja} :	~83 °C/W (Mounted on 4 layer PCB)
Θ _{jc} :	~16 °C/W
Lead Finish:	NiPdAu (e4)

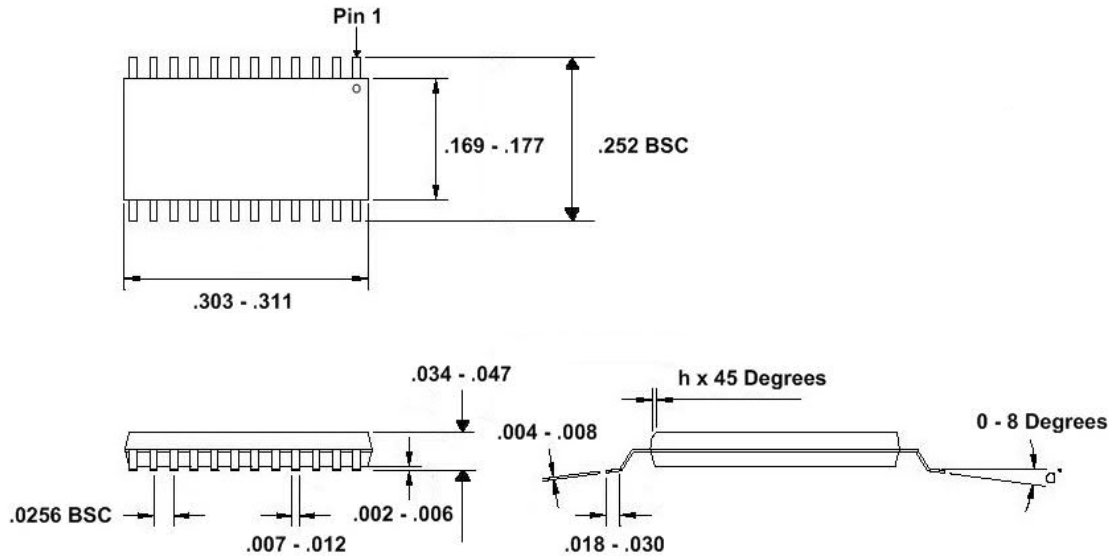


Figure 11 Outline Drawing

ORDERING INFORMATION

PART NUMBER	MARK	PACKAGE	TEMPERATURE
DEI1166-TES - G	DEI1166-TES e4	24 TSSOP	-55 / +85 °C
DEI1166-TMS - G	DEI1166-TMS e4	24 TSSOP	-55 / +125 °C

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