

# DEI1167

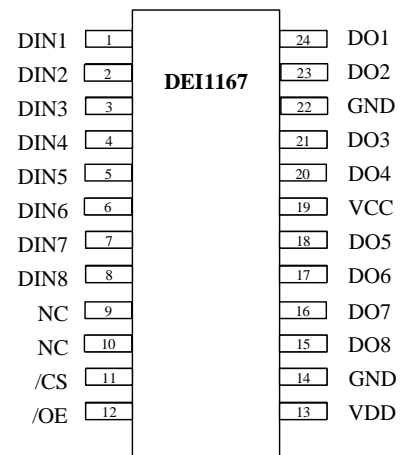
## OCTAL GND/OPEN INPUT, PARALLEL OUTPUT INTERFACE IC

### FEATURES

- Eight GND/OPEN discrete inputs
  - Meet electrical requirements for ABD0100 GND/OPEN discrete input.
  - Hysteresis provides noise immunity.
  - Internal pull up resistor
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160D, Section 22, Cat A3 and B3.
- 3.3V or 5V TTL/CMOS compatible digital IO
  - 8 tri-state outputs
  - /CS & /OE control inputs
- Logic Supply: 3.3V or 5V
- Analog Supply: 12V
- 24L TSSOP package

### PIN ASSIGNMENTS

**Figure 1 DEI1167 Pin Assignment**  
(24 Lead TSSOP)



**Table 1 Pin Descriptions**

Pins	Name	Description
8-1	DIN[8:1]	Discrete Inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The threshold and hysteresis characteristics are determined by the applied VDD voltage.
9-10	NC	Not Connected.
11	/CS	Chip Select Logic Input. Low input selects the device. Internal pull-up to VCC.
12	/OE	Output Enable Logic Input. Low input when /CS is low will enable the tri-state outputs. Internal pull-up to VCC.
13	VDD	Analog Supply. +12V
14	GND	Analog Ground.
19	VCC	Logic Supply. +3.3V or +5V
22	GND	Logic Ground.
15-18,20,21,23,24	DO[8:1]	Logic Outputs. Eight tri-state data outputs.

## FUNCTIONAL DESCRIPTION

The DEI1167 is an eight-channel parallel-output discrete-to-digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via a parallel 3-state output.

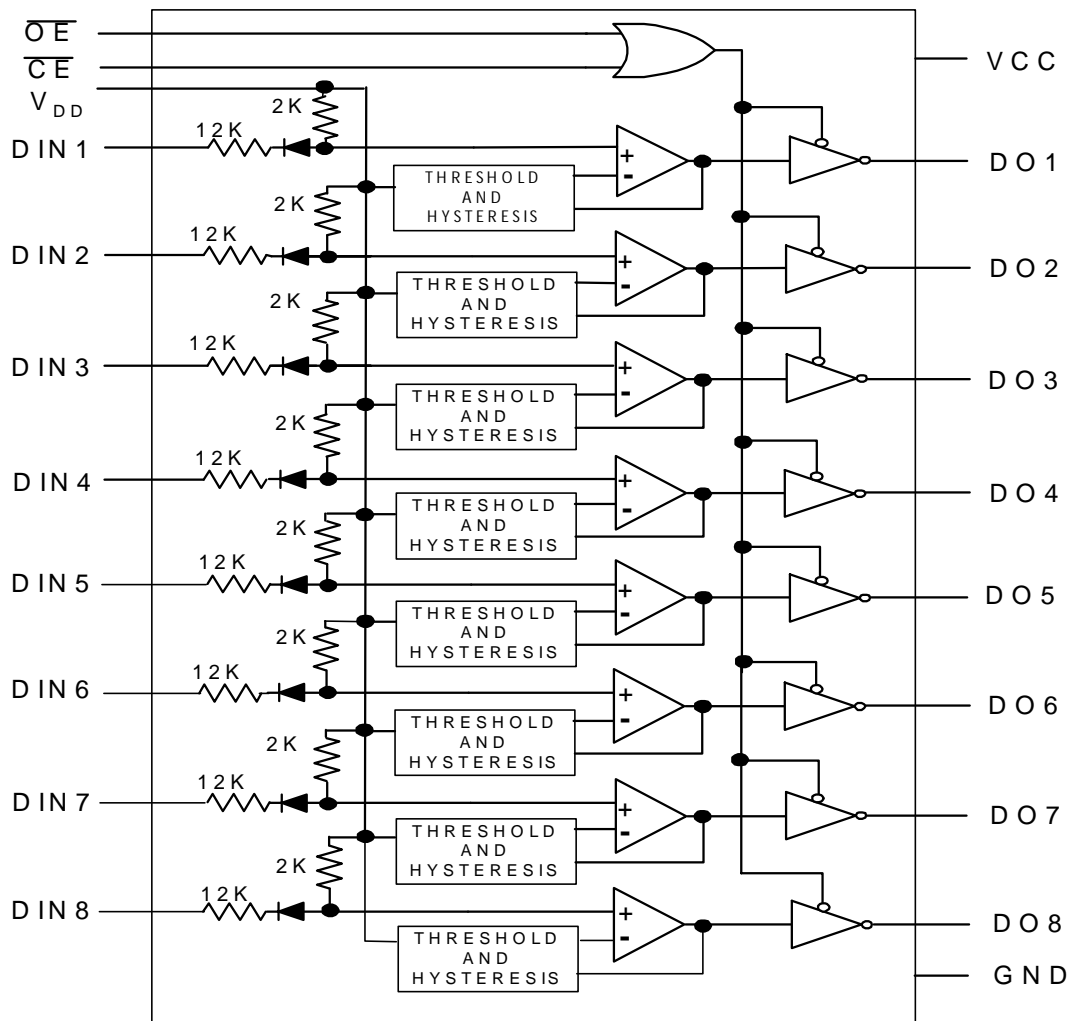


Figure 2 DEI1167 Function Diagram

Table 2 Truth Table

/CE	/OE	DIN[8:1]	DO[8:1]
L	L	Open	L
L	L	Ground	H
H	X	X	High Z
X	H	X	High Z

## DIN[8:1] INPUT STRUCTURE

Refer to Figure 2. Each DINn signal is conditioned by the resistor / diode network and presented to the comparator IN+. The reference and hysteresis voltage is developed at the comparator IN-. Notable features:

- When Vdd is +12V, the circuit shall source ~0.9mA to a grounded input. This current will prevent a “dry” relay contact.
- The input threshold voltage and hysteresis with Vdd = 12V ±10%:
  - The falling Vth > 3.5V
  - The rising Vth < 7.5V
  - Hysteresis > 1.5V
- The comparator includes an RC filter to provide noise rejection of transient pulses of up to several us. Thus there is a relatively large DINx setup time of several us (Refer to timing parameter tsu2).
- The inputs can withstand continuous input voltages of 40V minimum. The isolation diode breakdown voltage is greater than 50V. The 12K Ohm input resistor is designed to limit diode breakdown current to safe levels during transient events.

## TIMING DIAGRAMS

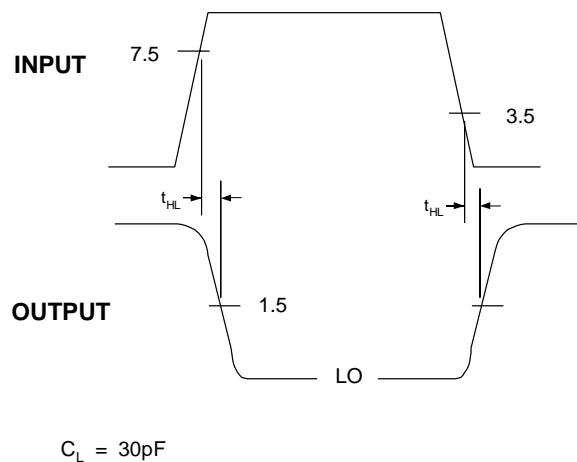


Figure 3 Input to Output Delay

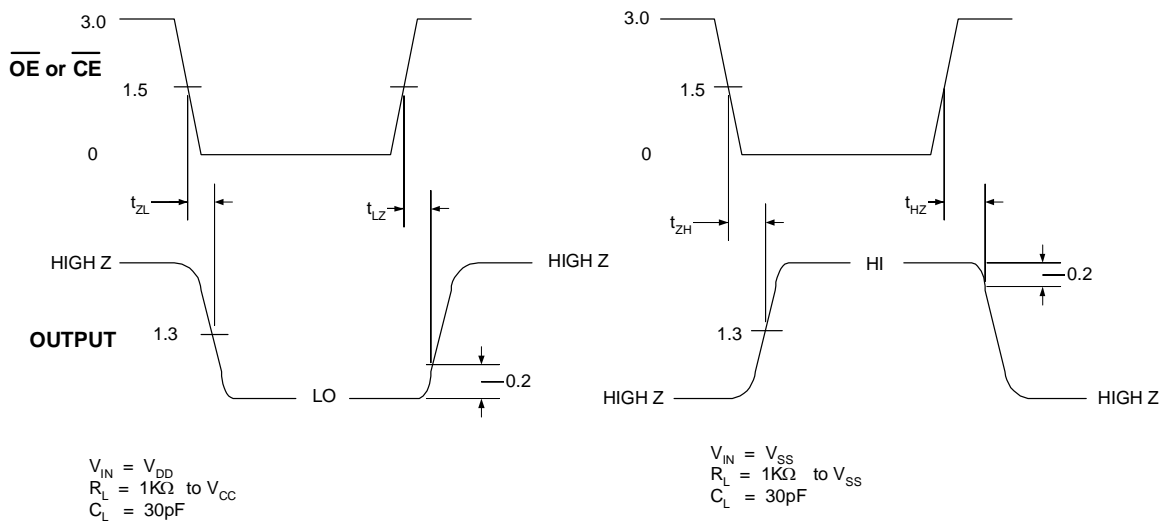
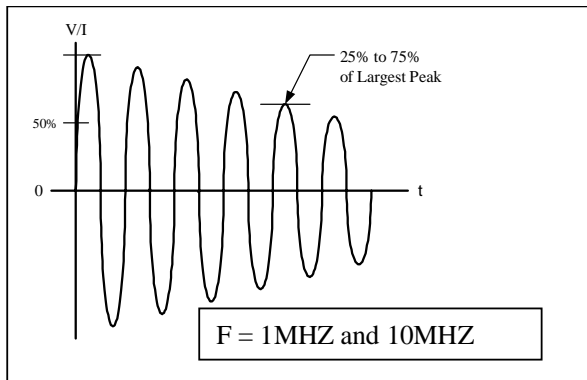


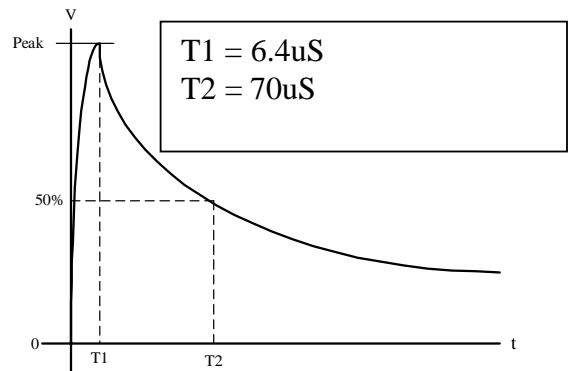
Figure 4 Chip Select or Output Enable to Output Delay

# LIGHTNING PROTECTION

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160D, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.



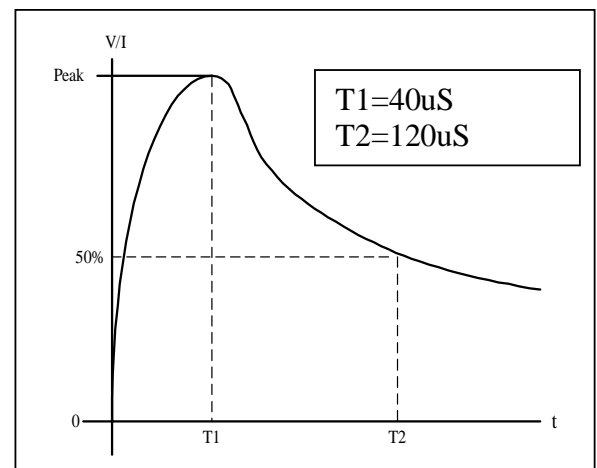
**Figure 5 Voltage / Current Waveform 3**



**Figure 6 Voltage Waveform 4**

Waveform Source Impedance characteristics:

- Waveform 3  $V_{oc}/I_{sc} = 600V / 24A \Rightarrow 25 \text{ Ohms}$
- Waveform 4  $V_{oc}/I_{sc} = 300 V / 60 A \Rightarrow 5 \text{ Ohms}$
- Waveform 5A  $V_{oc} / I_{sc} = 300V / 300A \Rightarrow 1 \text{ Ohm}$



**Figure 7 Current/Voltage Waveform 5A**

## ELECTRICAL DESCRIPTION

**Table 3 Absolute Maximum Ratings**

PARAMETER	MIN	MAX	UNITS
Vcc Supply Voltage	-0.3	+7.0	V
Vdd Supply Voltage	-0.3	20	V
Operating Temperature Plastic Package	-55	+125	°C
Storage Temperature Plastic Package	-55	+150	°C
Input Voltage			
DIN[8:1]      Continuous	-5	+40	V
DO160D, Waveform 3, Level 3	-600	+600	
DO160D, Waveform 4 and 5, Level 3	-300	+300	
Logic Inputs	-1.5	VCC + 1.5	
DO[8:1]	-0.5	VCC + 0.5	
Power Dissipation @ 85 °C: (> 10 Sec) 24L TSSOP		0.8	W
Junction Temperature: Tjmax, Plastic Packages		145	°C
ESD per JEDEC A114-A Human Body Model			
Logic and Supply pins		2000	V
DIN pins		1000	
Peak Body Soldering Temperature (10 sec duration)		260	°C
Notes:			
1. Stresses above absolute maximum ratings may cause permanent damage to the device.			
2. Voltages referenced to Ground			

**Table 4 Recommended Operating Conditions**

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC	5.0V±10%, 3.3V±10%
	VDD	12V±10%
Logic Inputs	/CS, /OE	0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40V
Operating Temperature		
	-TES	-55 to +85 °C
	-TMS	-55 to +125 °C

**Table 5 DC Electrical Characteristics**

Symbol	Parameter	Test Conditions	VCC (V)	LIMITS		Unit
				MIN	MAX	
LOGIC INPUTS AND OUTPUTS						
V <sub>IH</sub>	High level input voltage		3.6 5.5	2.0		V
V <sub>IL</sub>	Low level input voltage		3.0 4.5		0.8	V
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -20uA	3.0 4.5	VCC – 0.1		V
		I <sub>OH</sub> = -4.5mA	4.5	3.0		V
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20uA	3.0 4.5		0.1	V
		I <sub>OL</sub> = 4.5mA	4.5		0.40	V
I <sub>OZ</sub>	3-state leakage current	Output in Hi Impedance state. Vout = 0V and 5V	5.5	-10	+10	uA
I <sub>IIL</sub>	Low level input current	VIN = 0V	5.5	-300	-50	uA
DISCRETE INPUTS VDD = +12V						
V <sub>IH</sub>	High level input voltage		3.0 to 5.5	7.5		V
R <sub>IH</sub>	High level Din-to-GND resistance	Resistor from Din to GND to guarantee HI input condition	3.0 to 5.5	50K		Ohm
V <sub>IL</sub>	Low level input voltage		3.0 to 5.5		3.5	V
R <sub>IL</sub>	Low level Din-to-GND resistance	Resistor from Din to GND to guarantee LO input condition	3.0 to 5.5		500	Ohm
V <sub>Ihst</sub>	Input hysteresis voltage		3.0 to 5.5	1.3		V
I <sub>IH</sub>	High level input current	Vin = 7.5V	3.0 to 5.5	-420	-190	uA
I <sub>IL</sub>	Low level input current	Vin = 0V	3.0 to 5.5	-1.2	-0.6	mA
SUPPLY VOLTAGES VDD = +12V						
ICC	Quiescent logic supply current	Vin(logic) = Vcc or GND VIN[8:1] = open	5.5		800	uA
IDD	Quiescent analog supply current	Vin(logic) = Vcc or GND DIN[8:1] = Open	5.5		11	mA
		DIN[8:1] = GND	5.5		24	
Notes:						
1. Current flowing into DUT is positive. Current flowing out of DUT is negative. Voltages are referenced to GND.						

**Table 6 AC Electrical Characteristics**

Symbol	Parameter	VCC (V)	Limits		Unit
			-55 to 85°C	-55 to 125°C	
$t_{ZLmax}$ $t_{ZHmax}$	Maximum propagation delay, /CS↓ and /OE↓ to DO. (1) (3)	3.0 4.5 5.5	166 88 70	183 98 76	ns
$t_{HZmax}$ $t_{LZmax}$	Maximum propagation delay, /CS↑ or /OE↑ to DO HI-Z. from D0 Low or high. (1) (2) (3)	3.0 4.5 5.5	166 118 108	183 130 120	ns
$t_{HLmin}$ $t_{LHmin}$	Minimum data propagation delay, Din to DO (4) (5)	5.0	0.4	0.4	us
$t_{HImax}$ $t_{LHmax}$	Maximum data propagation delay, Din to DO (4) (5)	5.0	420	630	us
$C_{in-max}$	Maximum logic input Capacitance. (6)		10	10	pF
$C_{out-max}$	Maximum DO pin capacitance, output in HI-Z state. (6)		15	15	pF

Notes:

1. DO is loaded with 50pF to GND.
2. DO is loaded with 1K Ohms to GND for High output, 1K Ohms to VCC for Low output.
3. Timing measured from  $V_{IN}=1.5V$  to  $\Delta V_{OUT}=200mV$ . See Figure 4
4. See Figure 3
5. The delay is due to both the on chip filter circuits and VDD.
6. Guaranteed by design.
7. All measurements at VDD = 12V

**ORDERING INFORMATION**

Part Number	Marking	Package	Temperature
DEI1167-TES-G	DEI1167-TES	24 TSSOP	-55 / +85 °C
DEI1167-TMS-G	DEI1167-TMS	24 TSSOP	-55 / +125 °C

Note: Part is marked with "E4" after date code to denote lead free category

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# PACKAGE DESCRIPTION

## 24L TSSOP

Moisture Sensitivity:	Level 2 /260°C per JEDEC J-STD-020A (1yr floor life)
Θ <sub>ja</sub> :	84°C/W (Mounted on 4 layer PCB)
Θ <sub>jc</sub> :	16°C/W
Lead Finish:	NiPdAu plated
Materials:	RoHS compliant

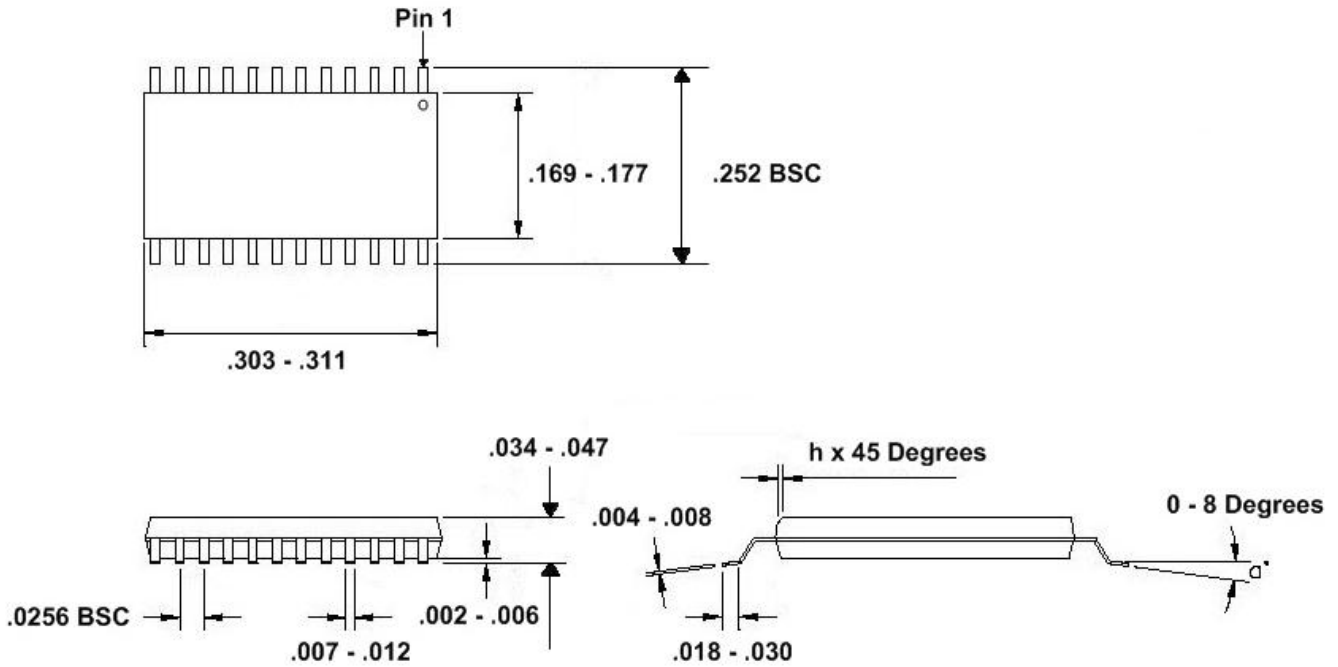


Figure 8 24 Lead TSSOP Outline Drawing